# 2018 XUP(Xilinx University Program) Professor Workshop Invitation

# 안녕하세요

Xilinx의 최신 기술 동향과 수업에 활용 가능한 새로운 교육코스를 교수님들께 전달하여 매번 큰 호응을 얻고 있는 Xilinx University Program Professor Workshop이 2018년 12월에 개최됩니다.

이번 워크샵은 Python Productivity for Zyng와 FPGA-based Accelerated Cloud Computing with SDAccel라는 각기 다른 주제로 Zyng SoC 의 기능을 활용 할 수 있는 오픈소스 프레임워크와 클 라우드기반의 가속화를 위한 SDAccel에 대해 소개합니다.

참가비는 무료이며 점심식사가 제공됩니다.

많은 관심과 참여 부탁 드립니다.

2018년 12월 6~7일, 오전 8시30분~오후 6시 ▶ 일시:

▶ 장소: 연세대학교

▶ 대상: Xilinx FPGA를 사용한 교육 및 개발에 관심이 있으신 대학교 교수님

▶ 인원: 20명

➤ 준비물: PYNQ-2 Board (Day 1)

\*제품 문의 : cho@libertron.com

▶ 신청: 홈페이지에서 사전 등록 (선착순 마감)

https://www.xilinx.com/support/university/workshops/korea-registration-form.html

| Day 1   | Day 2  |
|---|--|
| PYNQ: Pyhton Productivity on Zyng   | Introduction to AWS EC2 F1   |
| <ul> <li>Lab 1: Getting started with Jupyter<br/>Notebooks, Getting started with IPython,</li> </ul>      | - Lab 1: Connecting to AWS EC2 F1 lab  |
| Exploring PYNQ-Z2, Programming on-board   | SDAccel tools Overview   |
| peripherals   | - Lab 2: MakeFile Flow lab   |
| Introduction to Overlays  | SDAccel Flow   |
| <ul> <li>Lab 2: Working with Grove temperature<br/>sensor, PmodOLED, Grove LEDbar, Grove light</li> </ul> | - Lab 3 : GUI Flow lab   |
| sensor  | Optimization Techniques  |
| -   | - Lab 4 : Optimization lab   |
| <ul> <li><u>Logictools overlay</u></li> </ul>   |  |
|   | RTL Kernel Wizard  |
| IOP Architecture  | - Lab 5: RTL Kernel Creation lab   |
| - Lab 3: Wavedrom, BooleanGenerator,  |  |
| TraceAnalyzer, PatternGenerator lab<br>-  | <ul> <li>Debugging Techniques / Machine Learning</li> <li>Lab 6 : Debugging/Machine Learning in AWS</li> </ul> |
| Overlay Methodology   | EC2 F1 lab   |
| - Lab 4: MMIO, DMA, XLNK lab  |  |

## Course presented by

## Ph.D. Parimal Patel

Parimal received a Doctor of Philosophy in Electrical and Computer Engineering from the University of Texas at Austin, Texas in 1986.

In 1987 he joined the University of Texas as an Assistant Professor, got promoted to Associate and then to Full Professorships. During his tenure at the university he taught variety of courses including Logic Design, Digital Systems Design, Microcomputer Systems (peripheral interface principles), Embedded Systems Design, VLSI System Design, Computer Architecture, RISC Processor Design, Engineering Workstations, and Advanced HDL modeling.

Parimal has always enjoyed teaching and developing new courses. He started as a contract trainer and then full-time employee of Xilinx developing variety of courses for Customer Education department. He joined the Xilinx University Program in April 2007 developing new courses, updating current courses, and delivering XUP workshops worldwide, including High-Level Synthesis, Embedded Systems, Advanced Embedded Systems, DSP Design Flow, DSP Implementation Techniques, Designing with SDSoC, Dynamic Partial Reconfiguration, Python Productivity on Zynq (PYNQ), and Accelerated Cloud Computing on AWS with SDAccel.

문의사항이 있으시면 아래 담당자에게 연락하여 주시기 바랍니다.



부장 민혜영 Tel :02-3144-0249 helen.min@xilinx.com



팀장 오창훈 Tel: 010-6310-1135 <u>cho@libertron.com</u>