IDEC Chip Design Contest

D-band High Gain and Wide Bandwidth Low Noise Amplifier and Power Amplifier in 65nm CMOS Adopting Dual-Peak Gmax Technique

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Introduction

Issues of the D-band (110-170 GHz) Amplifier Design

- **Low maximum oscillation frequency (f_{max}) of CMOS transistors**
  - D-band is close to transistor's maximum oscillation frequency
  - Therefore, the intrinsic power gain (G_{ma}/G_{ms}, U) of transistor is low.

- **The number of stages of amplifiers**
  - Conventional amplifiers increase the number of stages to increase the power gain
  - As the number of stages increases, the power consumption increases.
  - In addition, the number of inter-stage matching network also increases, which degrades the gain per stage and bandwidth.

Circuit Description

Dual-peak G_{max}-based amplifiers

- **Dual-peak G_{max}-based 3-stage LNA**
  - Dual-peak G_{max}-core is adopted for high gain per stage and wide bandwidth.
  - 28um transistors are chosen by considering the gain per stage and minimum noise figure.
  - Source admittance (Y_S) is matched to optimum noise admittance ($Y_{n,opt}$) using input matching network.

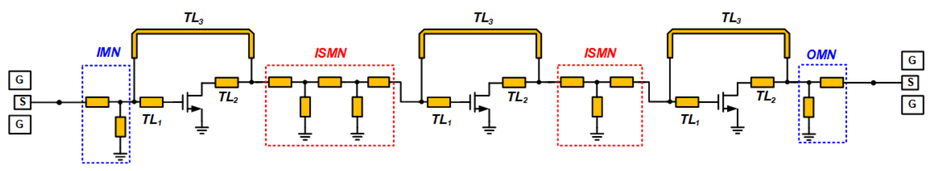

Fig.1 Circuit schematic of the dual-peak G_{max}-based 3-stage LNA

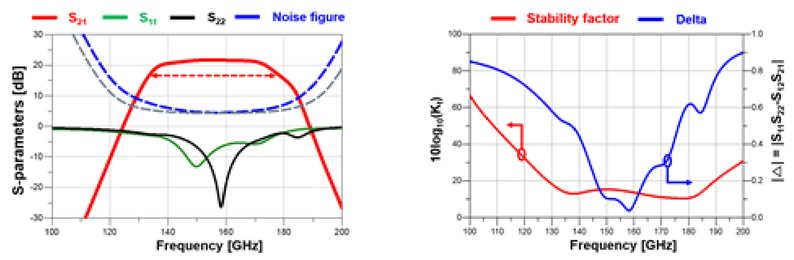

Fig.2 Simulation results of the dual-peak G_{max}-based 3-stage LNA

- **Dual-peak G_{max}-based 3-stage PA**
  - Dual-peak G_{max}-core is adopted for high gain per stage and wide bandwidth.
  - 28um transistors are chosen by considering the gain per stage, power consumption and linearity.
  - Load admittance (Y_L) is matched to optimum power admittance (Y_{opt}) using output matching network.

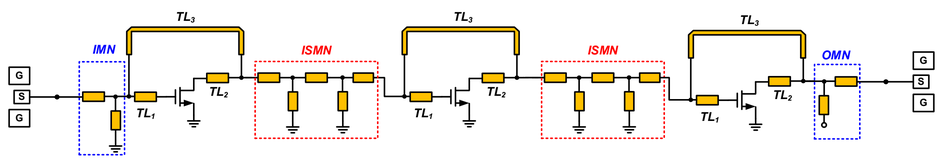

Fig.3 Circuit schematic of the dual-peak G_{max}-based 3-stage PA

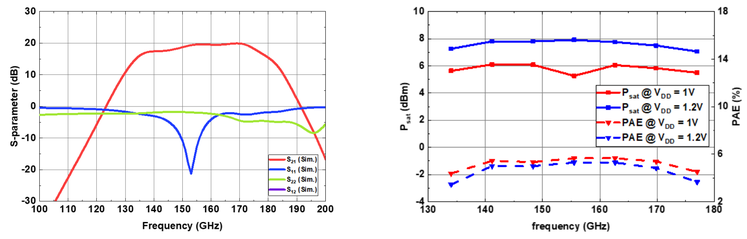

Fig.4 Simulation results of the dual-peak G_{max}-based 3-stage PA

Measurement Results

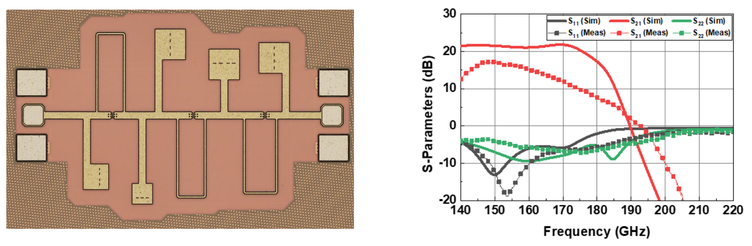

Fig.5 Chip photograph and measurement results of the LNA

References	This work	TMTT 21	IMS 12	TCAS-I 20	RFIC 21	TMTT 18	IMS 20	MWCL 19
Technology	40nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS	22nm SOI CMOS	28nm SOI CMOS	45nm SOI CMOS	130nm SiGe
f_{max} [GHz]	336	310	220	280	240	430	-	280
Topology	3 CS Stages	2 CS Stages	4 cascode Stages	8 CS Stages	6 CS Stages	4 CS Stages	8 CS Stages	2 cascode stages
f_o [GHz]	149.6 (154.5)*	152.2	117.5	120	150	160	135	143
Gain [dB]	17.2 (21.7)	17.9	25.3	20.6	15.5	15.7	16.1	16.1
BW_{3dB} [GHz]	22 (40)	11	18**	40.6	22	23	31.5	5**
NF [dB]	(4.4 – 7.2)	4.7 - 6.2	6-8.3	6.2	7.1 - 9.4	8.5	8	7
P_{DC} [mW]	18.0 (16.9)	13.7	48	45	28.8	32	75	36.8

* The simulation results are written in parentheses
** Estimated from graph

Table.1 LNA performance comparison table

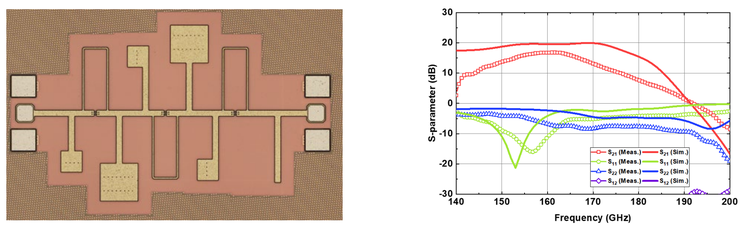

Fig.6 Chip photograph and measurement results of the PA

References	This work	EuMIC 20	RFIC 21	IEEE Access 21	IEEE Access 21
Technology	65nm CMOS	45nm CMOS SOI	45nm CMOS SOI	28nm CMOS	65nm CMOS
Topology	Dual-peak G_{max}-based CS	Neutralized diff.	Neutralized diff.	Neutralized diff.	G_{max}-based CS
# of Stages	3	4	4	3	2
Power Combining	X	X	8-way	2-way	X
f_0 [GHz]	159.5 (157.7)*	152.5	140	135	150
Gain [dB]	16.8 (19.9)	18	24	21.9	17.5
BW_{3dB} [GHz]	18.6 (40.6)	17.5	21	20	5
P_{sat} [dBm]	(6.3)	8.8	17.5	11.8	9.4
P_{DC} [mW]	98 (65.7)	92	410	140	52.4

* The simulation results are written in parentheses.

Table.2 PA performance comparison table

Conclusions

– By adopting the G_{max}-based amplifying stage with the optimum input and output matching network, the proposed LNA and PA are designed to have high gain per stage and widest bandwidth among the prior reported D-band amplifiers.
– However, due to the process variation and the inaccuracy of simulation tools in D-band, the fabricated chips' performance is degraded.
– Efforts to improve the accuracy of high-frequency simulations are needed to properly utilize the advantages of the G_{max} technique.

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