IDEC Chip Design Contest

High-Resolution Correlated Double Sampling Technique for High-Density Subretinal Implant

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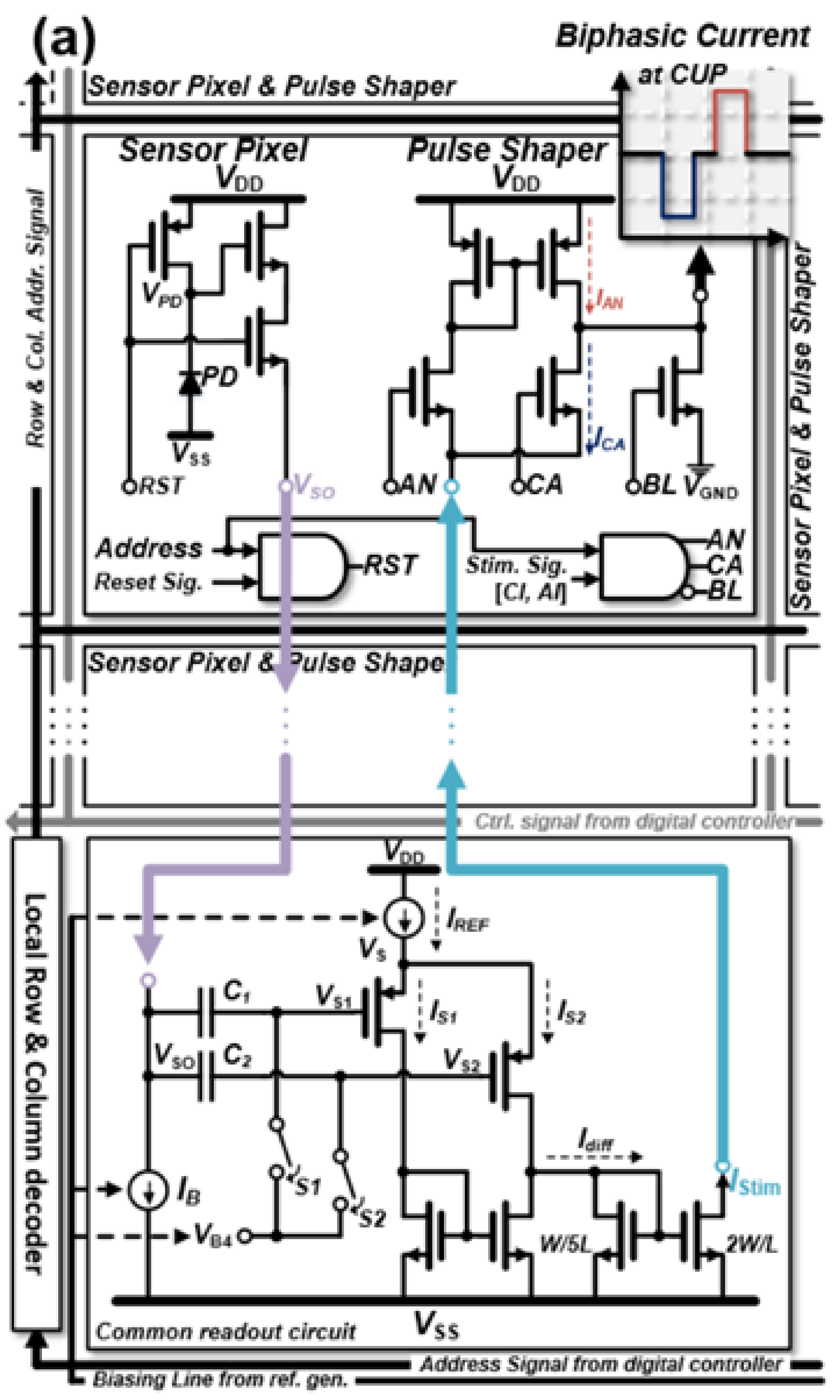
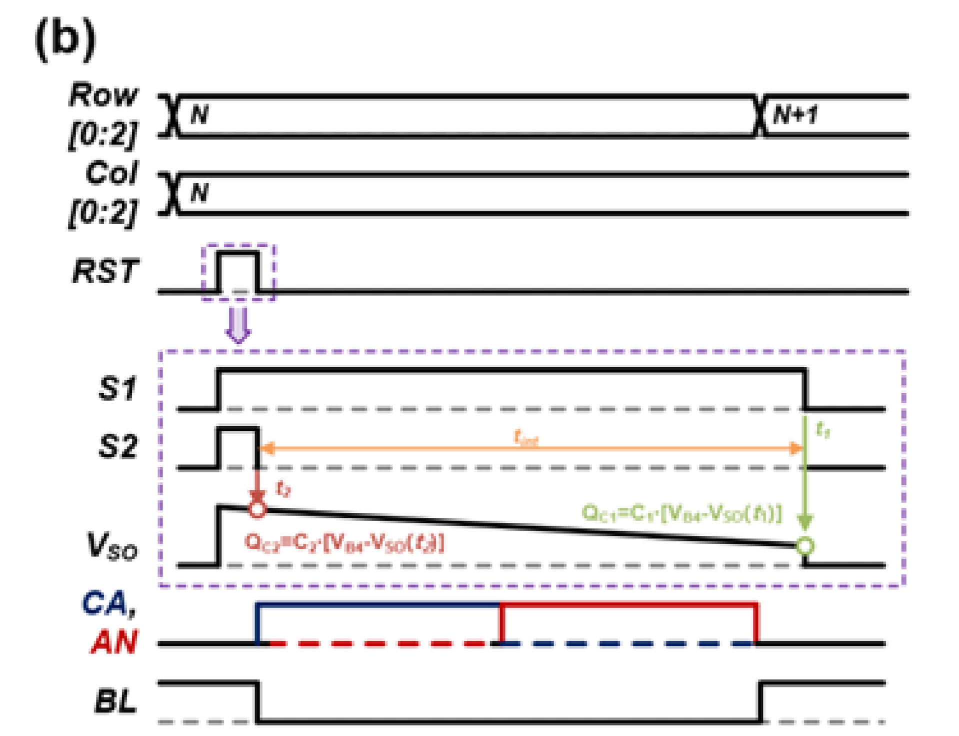
Introduction

This paper presents a 1,600-pixel integrated neural stimulator with a correlated double sampling readout (DSR) circuit for a subretinal prosthesis. The retinal stimulation chip inserted beneath photoreceptor layer is consisted with an array of active pixel sensor (APS) and biphasic pulse shaper. The experimental result shows that the proposed high-density stimulation array chip can accomplish high temporal resolution due to low integration time condition. The 1600-pixel retinal chip is designed and fabricated using a DB-HiTeK 0.18µm standard process.

Block Schematic Architecture

Fig. 1a shows schematics of the sensor pixel pulse shaper (SPPS) and the DSR circuit with address decoders. The address decoder determines which of SPPS is selected to connect with the DSR circuit, and is repeated after 25 sequences for cycling SPPSs. Fig. 1b illustrates a timing diagram of the SPPS and the DSR circuit in particular sequence of the cycle.





$$I_{diff} = I_{S2} - I_{S1} = g_m(V_S - V_{S2}) - g_m(V_S - V_{S1}) = g_m(V_{S1} - V_{S2})$$
$$= g_m\left({}^{Q_{C1}}/_{C_1} - {}^{Q_{C2}}/_{C_2}\right) = g_m\left(\frac{C_1\cdot[V_{B4}-V_{SO}(t_1)]}{C_1} - \frac{C_2\cdot[V_{B4}-V_{SO}(t_2)]}{C_2}\right)$$
$$= g_m[V_{SO}(t_2) - V_{SO}(t_1)] = g_m \cdot \left[\frac{I_{PD}}{C_{PD}}\cdot(t_1 - t_2)\right] = g_m \cdot \frac{I_{PD}}{C_{PD}} \cdot t_{int}$$
$$\therefore I_{Stim} = 10 \cdot g_m \cdot \frac{I_{PD}}{C_{PD}} \cdot t_{int} \quad where, V_{SO}(t) = A_{SF}\cdot\left(V_{dd} - \frac{I_{PD}}{C_{PD}}t\right)$$

Figure 1. (a) A schematic of the pulse shaper, and the CDS based readout circuit, which collaborated address signals from the digital controller, and bias from the reference generator. (b) A timing diagram on particular sequence that connected with the SPPS pixel; A I_{STIM}, a stimulus current amplitude is defined with a following equation under its timing diagram

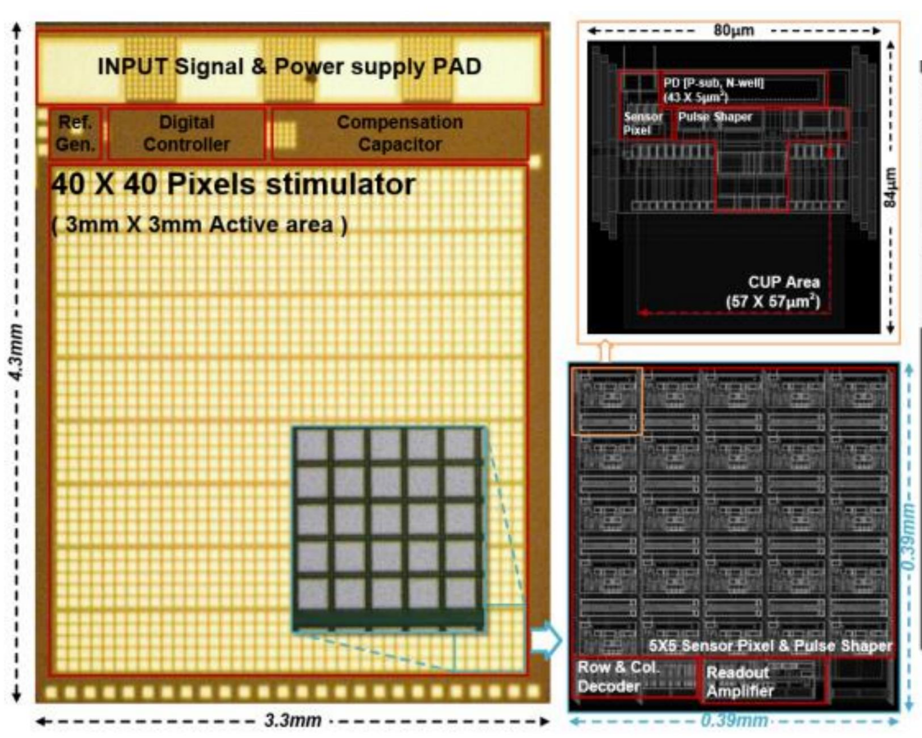


Figure 2. A microscopic image of the retina chip

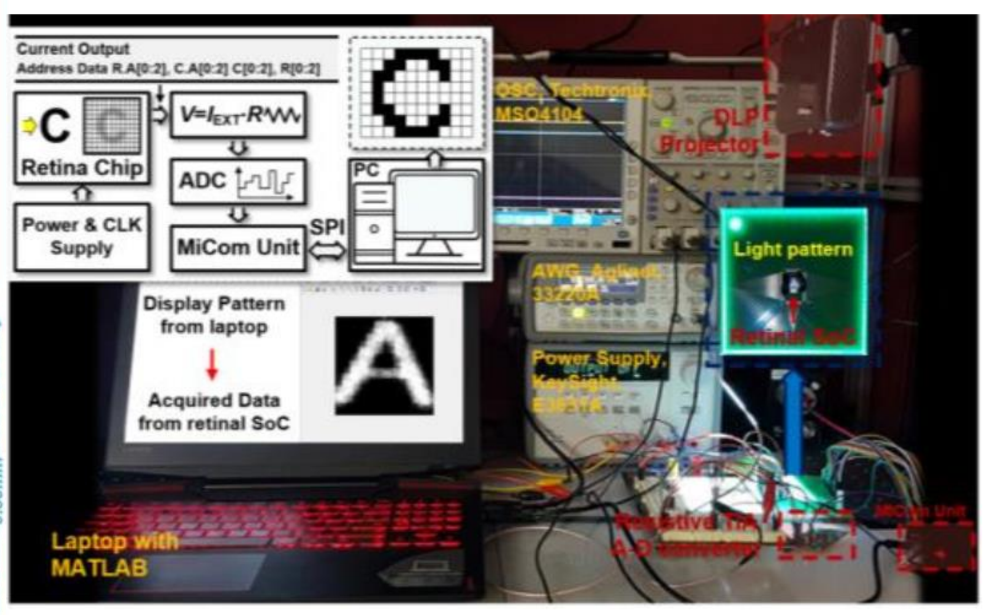


Figure 3. A demonstration bench for the proposed retina chip,

Experimental Results

		This Work	TBioCas'20[1]	TBioCas'21[2]
Sensor Pixel	APS	3Tr-APS	FPM	PWM
	Pwr/Ch	1.98µW	56.3nW	4.49nW
	Cur.Dev	≤ 0.63µA	≤ 3µA	≤ 6.175µA
Pulse Shaper	Pwr. $_{MAX}$/Ch.	10.8µW	1.45µW	4.28µW
	Comp. V	± 2.35V	± 1.6V	1V
	I_{STIM}	≤ 60µA	≤ 1mA	≤ 95µA
	t_{STIM}	≥ 1.152ms	-	≤ 15ms
	Cur. Dev.	≤ 0.51µA	-	≤ 0.475µA
Area	Pixel Size	84× 80.3µm²	84× 86.6µm²	90× 60µm²
	Total Size	4.3×3.3 mm²	5×3.45 mm²	2.93×2.55 mm²

Table 1. Performance of proposed system

Conclusion

This paper presents high-temporal and high-spatial resolution neural stimulator to achieve non-flicker and high-resolution visual restoration. The proposed retina chip with 1600 stimulation pixels is implemented with the DSR circuit that works to recognize a light intensity in short integration time. In addition, with considering the mismatch on the Monte-Carlo simulation, the retina chip attains smallest standard deviation of the current output compared with conventional retina chips.

Acknowledgement

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Reference

[1] J. H. Park, J. S. Y. Tan, H. Wu, Y. Dong and J. Yoo, "1225-Channel Neuromorphic Retinal-Prosthesis SoC With Localized Temperature- Regulation," in IEEE Transactions on Biomedical Circuits and Systems, vol. 14, no. 6, pp. 1230-1240, Dec. 2020.

[2] D. -H. Choi, H. Roh, M. Im and D. -W. Jee, "A 4.49nW/Pixel Light-to- Stimulus Duration Converter-Based Retinal Prosthesis Chip," in IEEE Transactions on Biomedical Circuits and Systems, vol. 15, no. 6, pp. 1140-1148, Dec. 2021.

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