IDEC Chip Design Contest



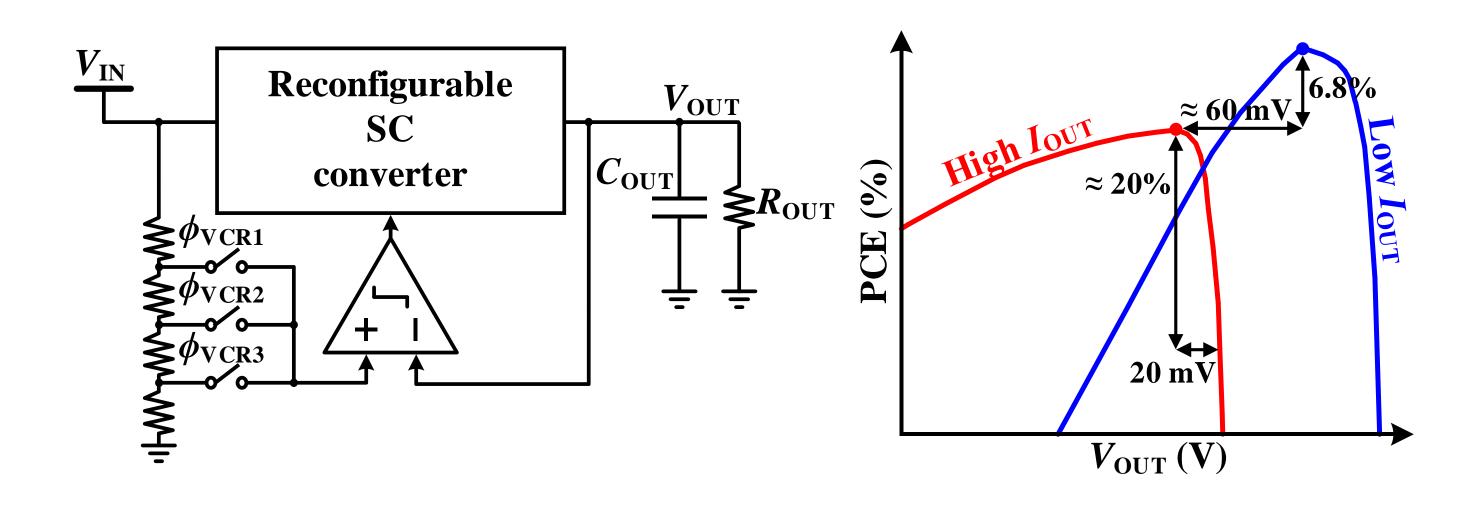
2023 IDEC CDC - HM - 2102

An Overlapped-Conversion-Ratio Modulation for Tri-Loop 3-D Reconfigurable SC Feedback Network

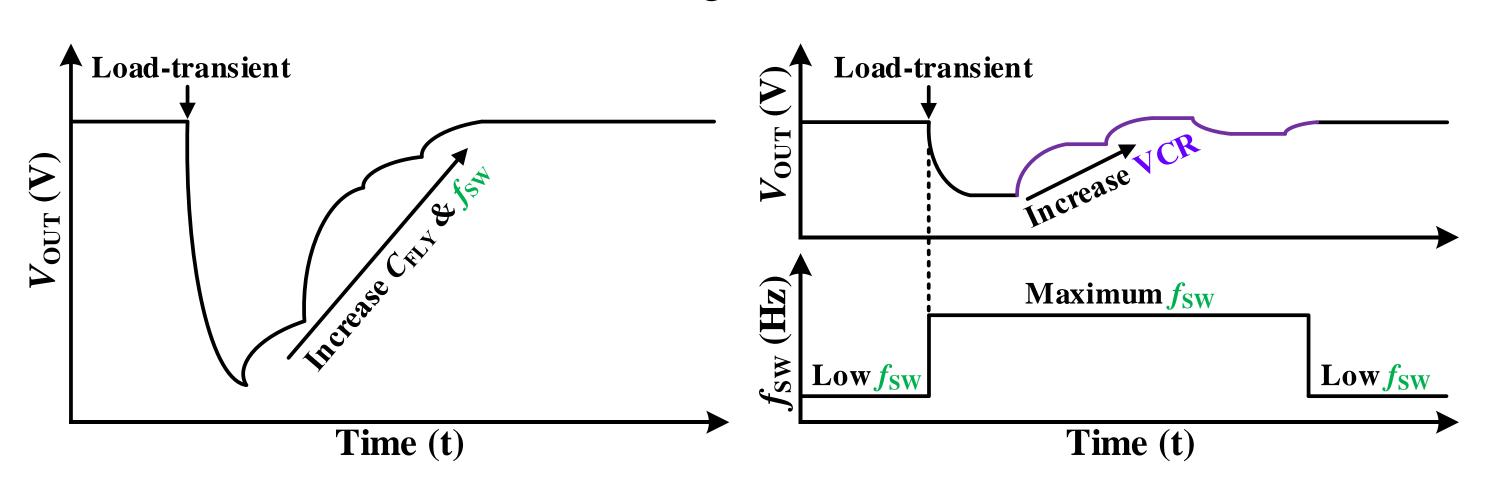
Hyunjin Kim, Taehyeong Park, and Chulwoo Kim Korea University, Seoul, Korea

Conventional Feedback Network

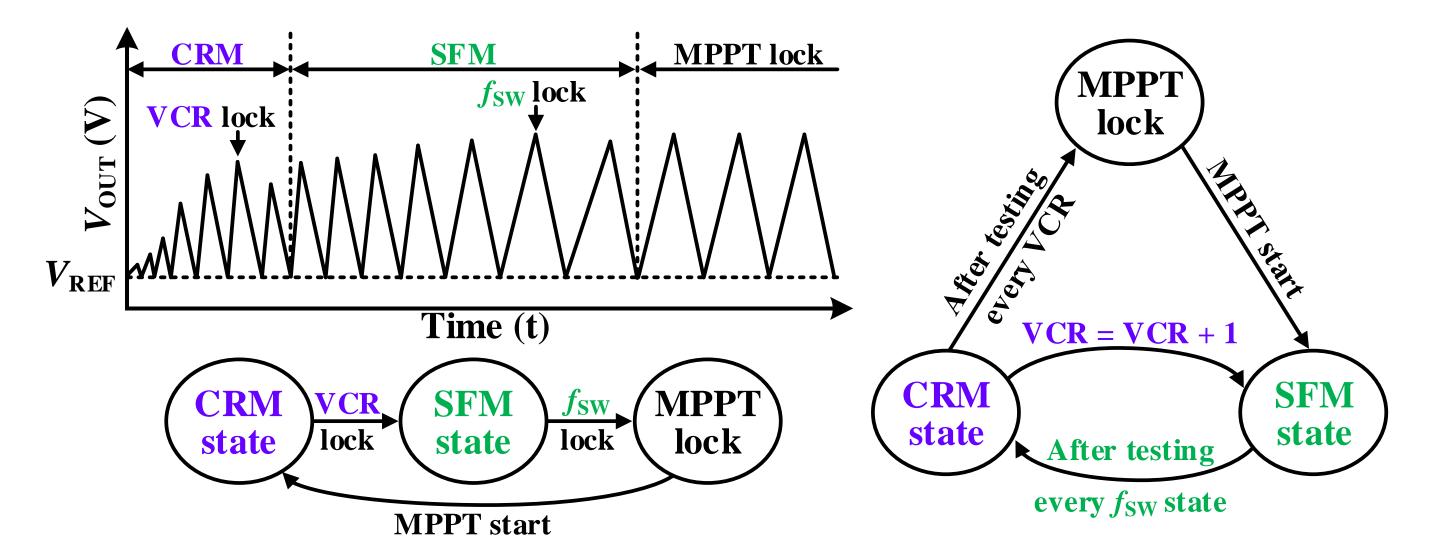
* Conventional fixed conversion ratio modulation (CRM) scheme



* Conventional fast transient tracking schemes

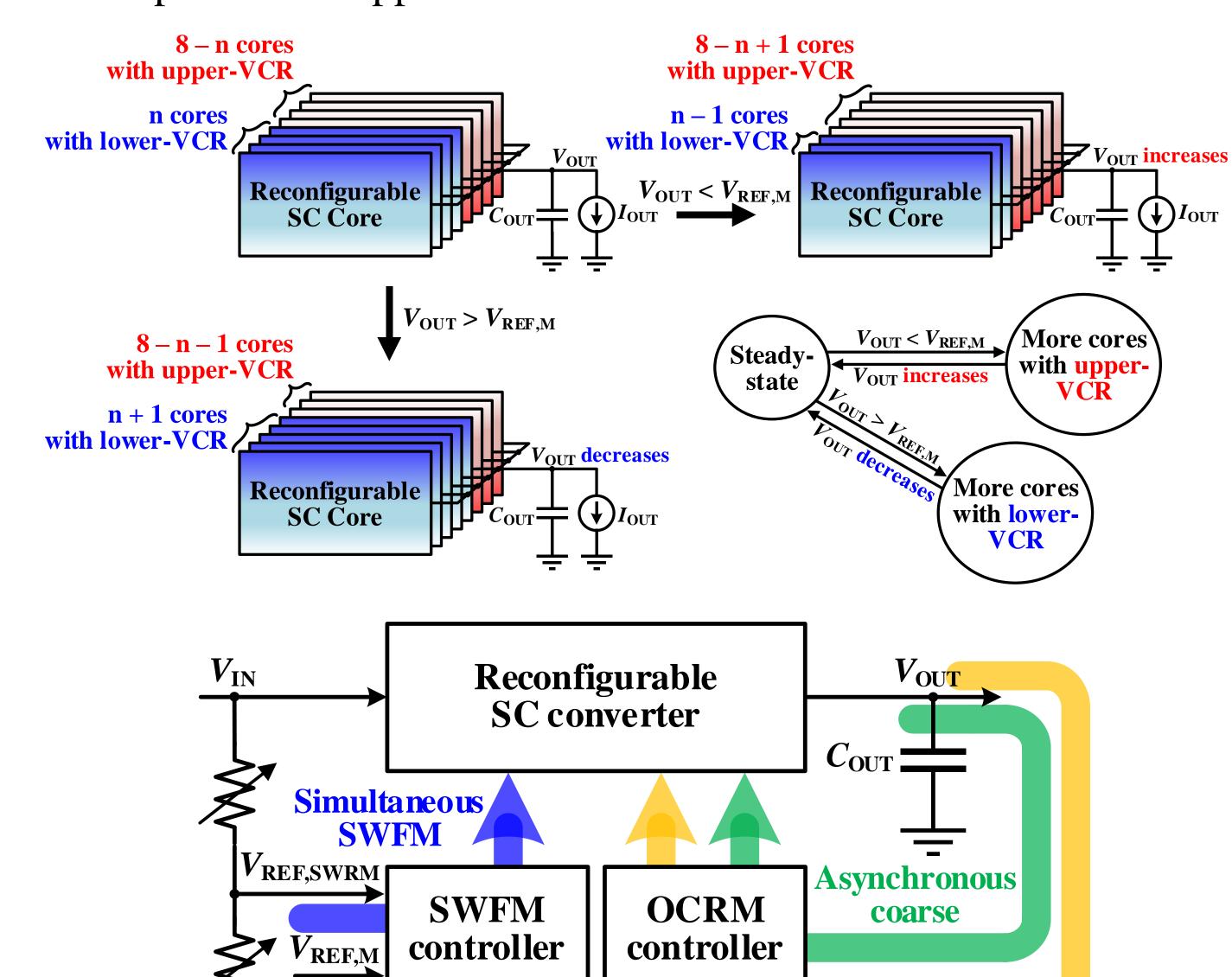


* Conventional SC converter MPPT schemes



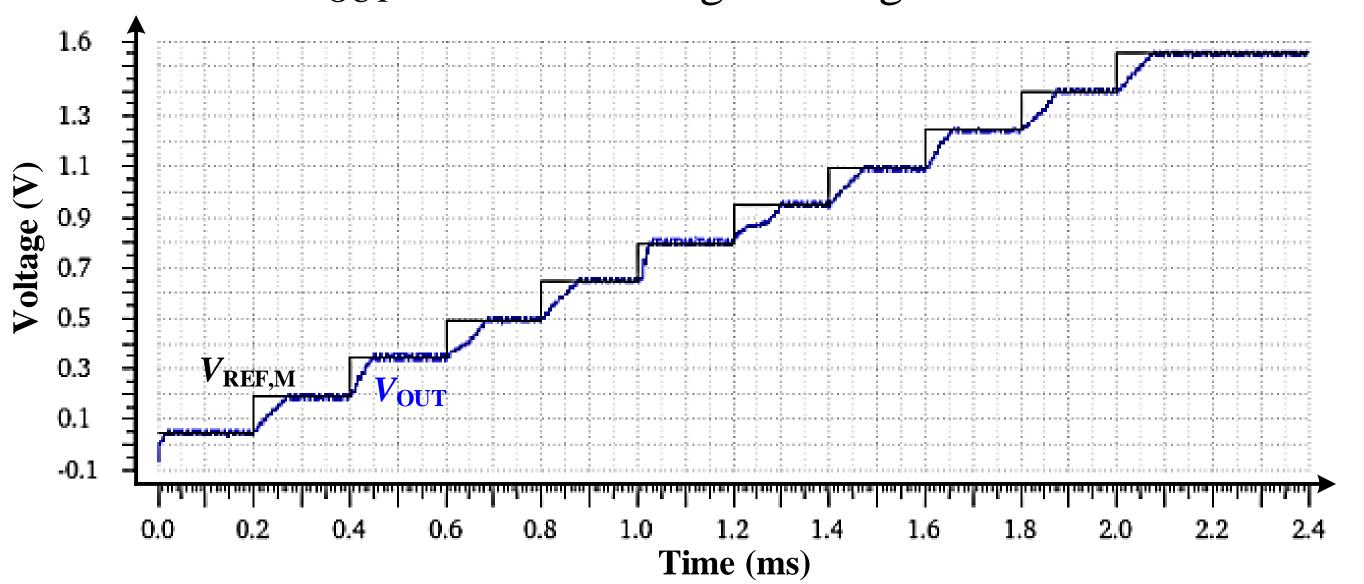
Proposed Feedback Network

* Proposed overlapped-CRM scheme

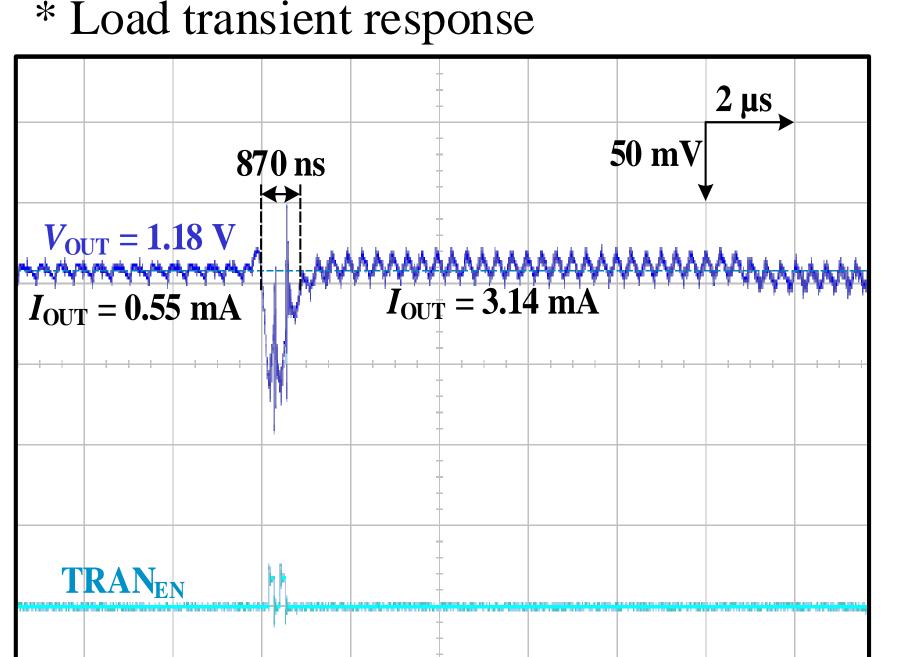


* Simulated V_{OUT} waveform using reconfigurable SC converter

Synchronous fine



Measurement Results



* Dynamic voltage scaling $R_{\rm OUT} = 630 \, \Omega$ $V_{\text{OUT}} = 1.38 \text{ V}$ 20 μς $V_{\text{OUT}} = 1.09 \text{ V}$ 100 mV

Acknowledgement: The chip fabrication and Electronic Design Automation (EDA) tool were supported by the IC Design Education Center (IDEC), Daejeon, South Korea.

TRANEN

	Liu, ISSCC'15	Salem, ISSCC'14	Rawy, ASSCC'17	Cheng, TCAS1'20	This Work
Technology (nm)	180	250	65	180	180
Topology	Monolithic SC	4-b SC	SPSC	SPSC	SPSC
Feedforward control	N/A	N/A	CRM	CRM	N/A
Feedback control	CRM → SFM	CRM → SFM	SFM & SWM	SFM & PSM	CRM & SFM & SWM
Seamless CRM	No	No	No	No	Yes
Fully-integrated	Off-chip C _{OUT}	Off-chip C _{OUT}	Off-chip C _{OUT}	Off-chip C _{OUT}	Yes
$V_{\mathrm{IN}}\left(V\right)$	0.45-3	2.5	0.35-1	0.53-0.7	1.8
V _{OUT} (V)	3.3	0.1–2.2	1	1.2	1.05-1.45
# of VCRs	14	15	6	3	5
Interleaving phase	1	1	1	4	8
Settling time (µs)	208	8	0*	34	0.87
Peak PCE (%)	81	85	88	80.8	80.2
PCE _{OL} -PCE _{CL} (%)	8	NR	NR	NR	0.2-1.9
P _{OUT} (µW)	< 50	30–4940	0.1-300	9–63*	<3700
C _{FLY} (nF)	N/R	3	0.24	2.62	2.8
Active area (mm ²)	4	4.645	0.54	4.04	2.84

* Only small I_{OUT} step response (w/o CRM) is reported ** C_{OUT} included

