IDEC Chip Design Contest

A Process-scalable Ultra-low-voltage 180kHz Sleep Timer with Time-domain Amplifier and Switch-less Resistance Multiplier

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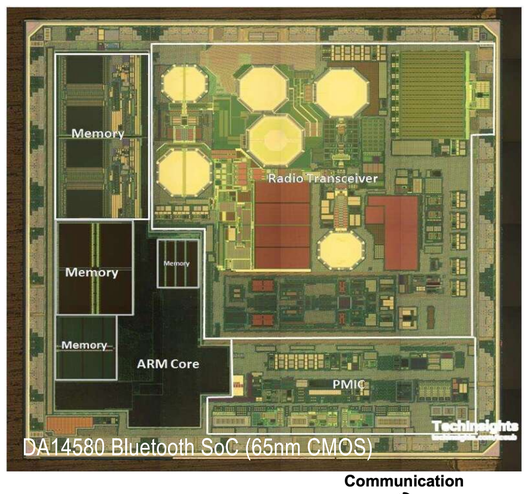
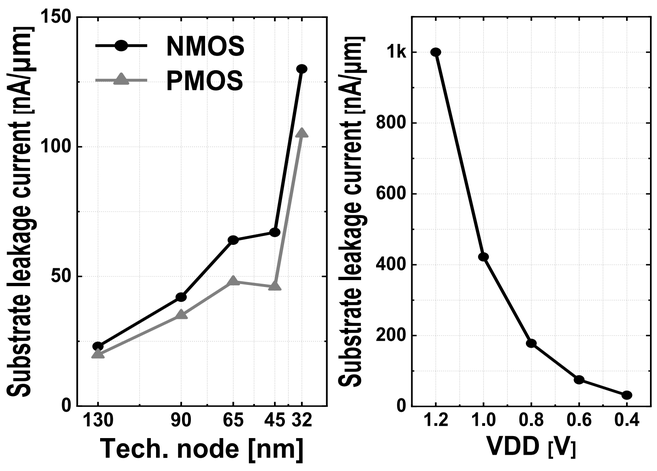
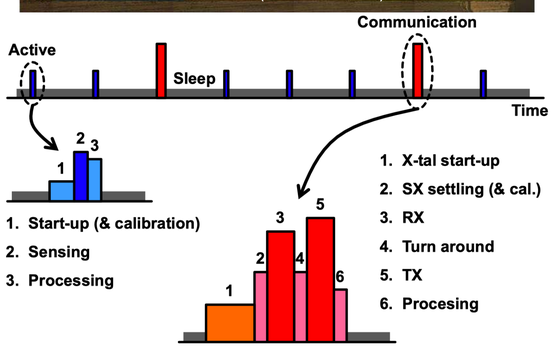
Abstract

An energy-efficient precise on-chip sleep timer is a key enabler of wireless SoCs for IoT. Having a lookup-table (LUT) with a temperature sensor (TS) for calibration is inevitable to accomplish the high accuracy required by wireless sensor nodes. Thus, the sleep timer's intrinsic temperature dependency determines the energy efficiency of the overall sleep timer system. On-chip sleep timers suffer from various leakages that exponentially increase with temperature. Moreover, the process scaling also increases the leakages exponentially. In this paper, we present a process-scalable kHz-range on-chip sleep timer. Our sleep timer overcomes the limitations of conventional on-chip sleep timers by using a combination of ultra-low-voltage (ULV) frequency-locked loop (FLL) architecture, a time-domain amplifier (TDA), and a gate-leakage leveraging technique. Our sleep timer, fabricated in TSMC 65nm MSRF GP process, produces 180kHz frequency with 61nW power consumption at 0.4V supply. Our sleep timer achieves 2.73ppm/°C temperature dependency with LUT-based calibration.

Sleep Timer in Duty-Cycled Wireless SoCs

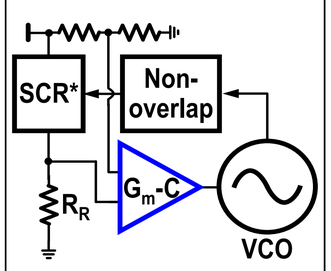
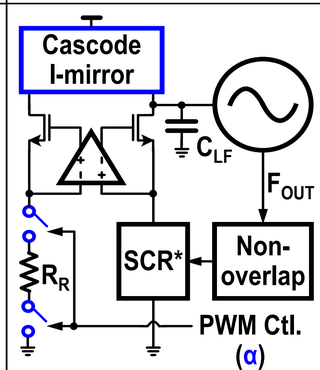
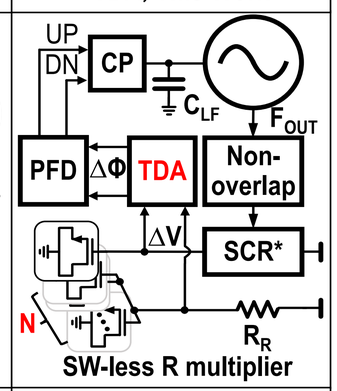






- Duty cycling: key in ultra-low-power wireless systems
  - Good sleep timer performance is required
- Process scaling
  - Pros: SoC cost, speed, and energy-efficiency
  - Cons: Difficulty in sub-μW analog design
    - ✓ Exponential increase of leakages with process scaling
- **This work**: **process-scalable ultra-low-voltage sleep timer**

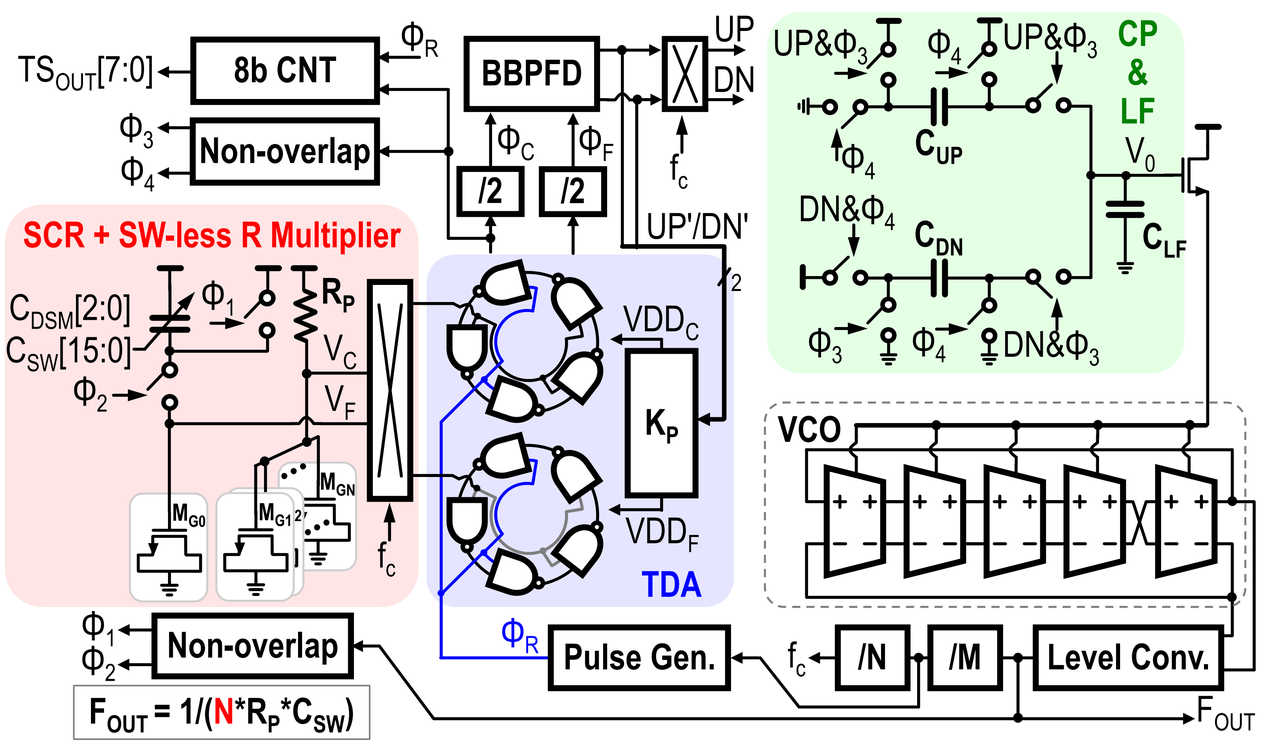
Process-scalable FLL Architecture

F2V + Analog Gm-C [A. Khashaba, ISSCC' 20]	F2I + Current Mirror [G. Cristiano, SOVC' 20]	F2V + SW-less R Multiplier + TDA, This Work
		
65nm / 1.2V / 32MHz	180nm / 1.8V / 116kHz	65nm / 0.4V / 180kHz
No low-freq. technique	Switched R multiplier	SW-less R multiplier
$F_{OUT} = 1/(R_R C_{SCR})$	$F_{OUT} = \alpha/(R_R C_{SCR})$	$F_{OUT} = 1/(NR_R C_{SCR})$
LUT calibration, off-chip temp. sensor	LUT calibration, in-situ temp. sensor	LUT calibration, in-situ temp. sensor
34uW	694nW	61nW
Folded-cascode OTA	Cascode current mirror	Time-domain amplifier

*SCR(switched-capacitor resistor)

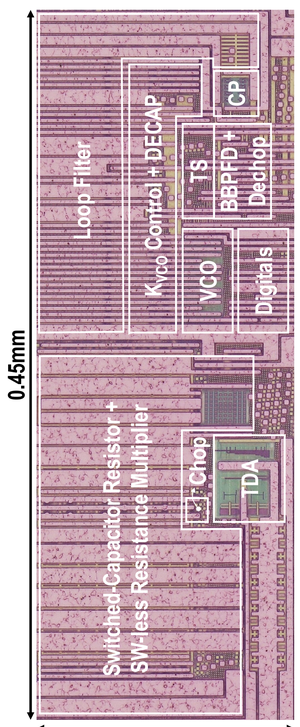
- Accuracy limited by leakages, exponentially increasing with process scaling
- R multiplication required to implement an energy-efficient low-frequency sleep timer
- ULV architecture required to minimize leakages, exponentially increasing with VDD

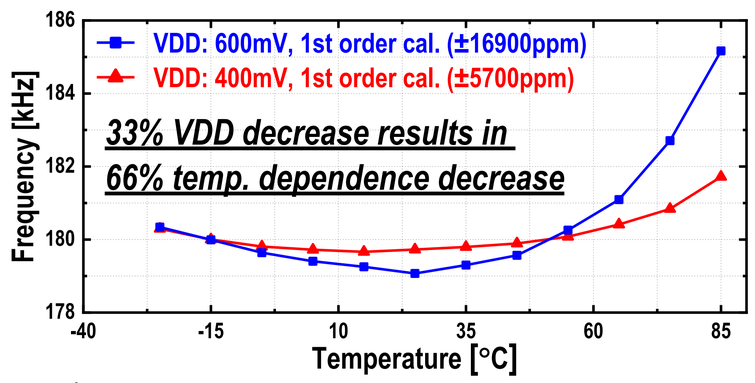
Process-scalable ULV Sleep Timer

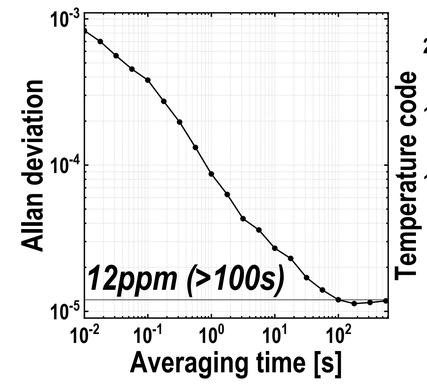


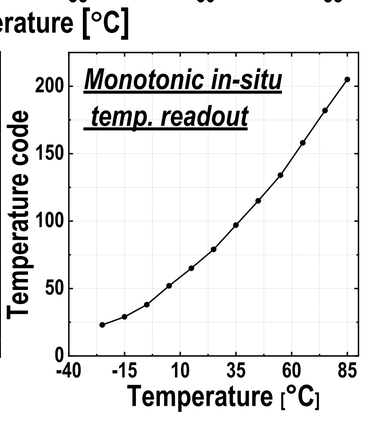
- **Switch-less resistance multiplication** by using a gate-leakage divide pair
- **Time-domain amplifier (TDA)** using a gated-VCO pair
  - Voltage difference amplified into the phase difference
  - TDA also used for in-situ temperature sensing
- **ULV charge pump** using switched capacitors

Measurement Results & Die Micrograph









Comparison & Conclusion

	Process [nm]	Supply [V]	F_{OUT} [kHz]	Power [nW]	Current efficiency [nA/cycle]	Area [mm²]	TC [ppm/°C]	Allan dev. [ppm]	Temp. range [°C]	In-situ temp. sensor	FLL reference	Low F_{OUT} technique
ISSCC20 Gürleyük	180	1.8	16,000	400,000	13.89	0.3	6.15	0.32 (>10s)	-45 to 85	Yes (analog)	Wheatstone bridge	-
ISSCC20 Khashaba	65	1.2	32,000	34,000	0.89	0.18	8.4	2.5 (>2.5s)	-40 to 85	No	Resistor divider	-
VLSI20 Ding	40	1	428	380	0.89	0.07	8	10 (>100s)	-40 to 80	Yes (digital)	Resistor	-
VLSI20 Cristiano	180	1.8	116	694	3.32	1.2	8.7	4 (>100s)	-15 to 85**	Yes (digital)	Resistor	Switched resistor
ISSCC16 Jang	180	1.1	3	4.7	1.42	0.5	13.8	63 (>100s)	-25 to 85	No	Resistor	Switched resistor
VLSI 18 Lim	55	1.2	0.09	0.224	2.07	0.06	260	177 (>100s)	-5 to 95	Yes (analog)	Gate-leakage	Gate-leakage reference
This Work	65	0.4	180	61	0.85	0.08	2.73*	12 (>100s)	-25 to 85**	Yes (digital)	Resistor	Gate-leakage pair

- Process-scalable ULV sleep timer for the first time
- Current efficiency maintained for output frequency < 200kHz
- In-situ temperature sensing for calibration at the system level

Acknowledgement

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