IDEC Chip Design Contest

A 13-bit Pipelined-SAR ADC for Mobile IoT Devices

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Introduction

- Some mobile IoT devices incorporate high-resolution sensors and operate within a limited bandwidth of a few Mega-Hertz. For such applications, a pipelined-SAR analog-to-digital converter (ADC) is typically used to convert analog signals in nature into digital signals. [1]
- A pipelined-SAR ADC consists of multiple SAR ADCs, where a residue amplifier amplifies the residue signal in the coarse-stage ADC with a certain inter-stage gain. The digital outputs are combined through error correction.

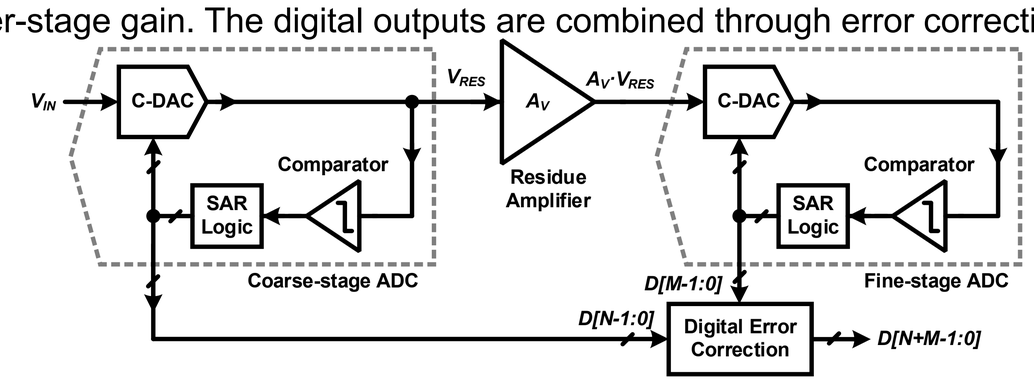

Fig. 1. Block diagram of a pipelined-SAR ADC

Top Block Diagram

- Fig. 2 represent overall block diagram of the presented 13-bit pipelined-SAR ADC. The ADC is designed differentially in actual implementation.
- A residue amplifier amplifies coarse-stage residue signal with 8 V/V gain.
- C-DACs are implemented with a split-capacitor technique to reduce switching energy and maintain same top-plate common-mode level during comparisons.
- A global SAR logic synchronously controls the overall ADC's operation.

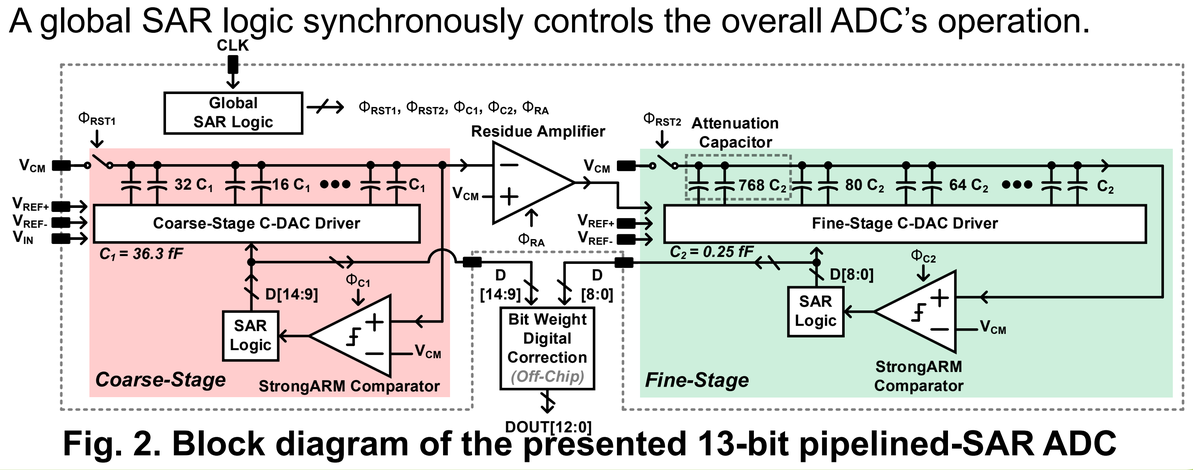

Fig. 2. Block diagram of the presented 13-bit pipelined-SAR ADC

Measurement Results

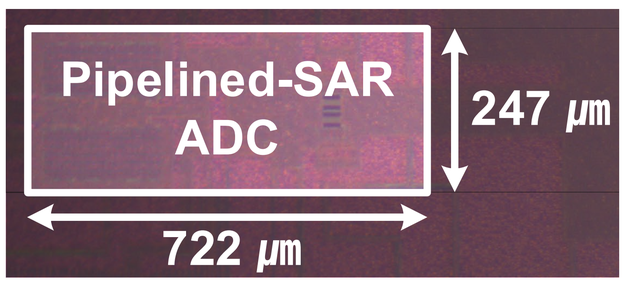

Fig. 3. Chip Microphotograph

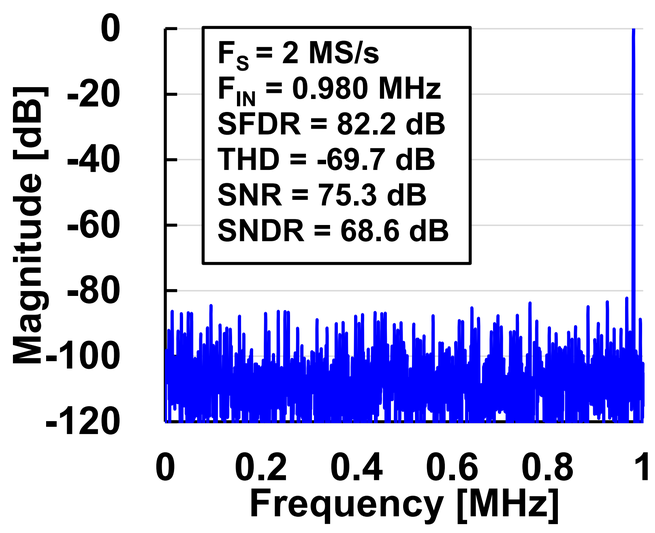

Fig. 4. ADC output spectra at F_S = 2MS/s

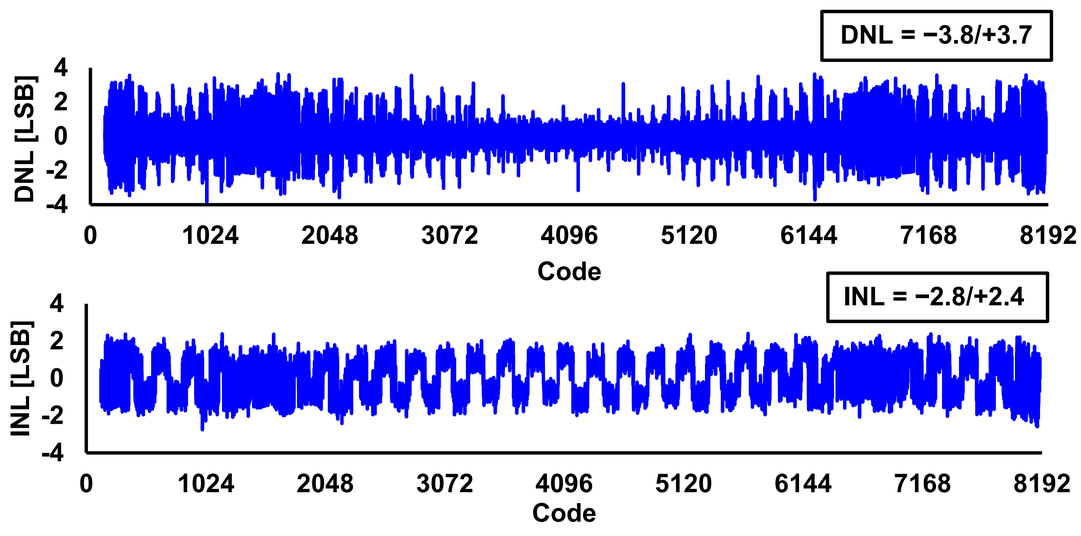

Fig. 5. ADC's DNL and INL

- Fig. 3. represents the microphotograph of the fabricated pipelined-SAR ADC in 65 nm CMOS technology. It occupies total area of 0.18 mm^2 and active area of 0.023 mm^2.
- Fig. 4. displays the ADC's dynamic performance at sampling frequency (F_S) of 2 MS/s. The ADC achieves 68.6 dB signal-to-noise-and-distortion ratio (SNDR) and 82.2 dB spurious-free dynamic range (SFDR).
- Fig. 5. shows the ADC's differential non-linearity (DNL) and integral non-linearity (INL). The maximum DNL and INL are 3.8 LSB and 2.8 LSB, respectively.
- Table I summarizes the ADC's performances. The ADC consumes 72.3 μW, and achieves FoM_{SNDR} of 170.0 dB and FoM_{SNR} of 176.7 dB.

TABLE I. ADC Performance Summary

Parameter	Value	Parameter	Value
Process	65 nm CMOS	SFDR	82.2 dB
Fs	2 MS/s	THD	-69.7 dB
V_{DD}	1.2 V	SNR	75.3 dB
Power	72.3 μW	SNDR	68.6 dB
Area (Active)	0.18 mm^2 (0.023 mm^2)	FoM_{SNR}*	176.7 dB
		FoM_{SNDR}**	170.0 dB

* FoM_{SNR} = SNR + 10 × $\log_{10}$(F_S / (2×Power))
** FoM_{SNDR} = SNDR + 10 × $\log_{10}$(F_S / (2×Power))

Summary & Conclusion

- A 13-bit 2 MS/s pipelined-SAR ADC for mobile IoT devices is fabricated in 65nm CMOS process.
- The ADC achieves SNDR of 68.6 dB and FoM_{SNDR} of 170.0 dB at F_S = 2 MS/s. The SNDR performance is limited by total-harmonic distortions (THD) of -69.7 dB as shown in Fig. 4, and also limited by non-linearities as shown in Fig. 5.
- The ADC can perform better energy efficiency by calibrating the non-linearities in the future work, since FoM_{SNR} shows better performance of 176.7 dB.

Acknowledgement

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References

[1] X. Tang, X. Yang, J. Liu, W. Shi, D. Z. Pan and N. Sun, "27.4 A 0.4-to-40MS/s 75.7dB-SNDR Fully Dynamic Event-Driven Pipelined ADC with 3-Stage Cascoded Floating Inverter Amplifier," 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 376-378.