IDEC Chip Design Contest



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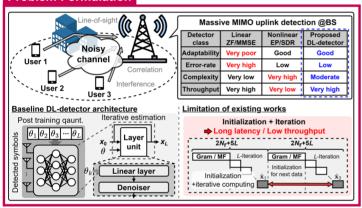


Abstract

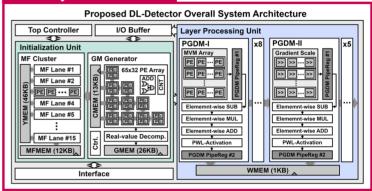
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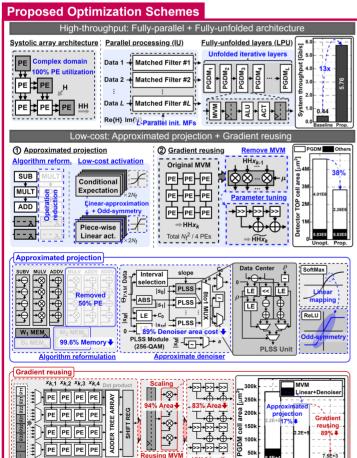
This work presents the first fabricated massive deep-learning (DL) multiple-input multiple-output (MIMO) detector for a 128×32 antenna configuration and 4 to 256QAM modulations, offering near-optimal detection across diverse channel conditions. Our design employs the fully parallel initialization procedure followed by the fully unfolded DL operations, enhancing the data rate by 13 times compared to the baseline design. We also propose a novel approximate projection to relax the processing cost per layer and a gradient reusing to eliminate all the matrix-vector multiplications (MVMs) in the last few layers, saving the overall detector complexity by 38%. Targeting the 256QAM system, our prototype in a 28nm CMOS process offers a throughput of 5.76 Gb/s and an energy efficiency of 79.7 pJ/b, surpassing the previous state-of-the-art detectors.

Problem Formulation



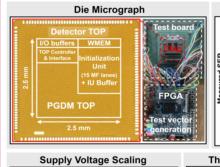
Overall System Architecture

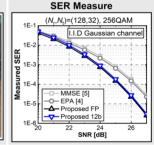


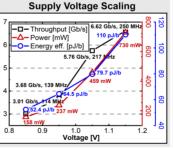


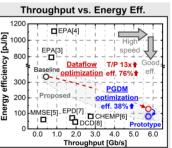
Implementation Results

Measurement results









Comparison to other state-of-the-art detectors

Detector	I his work	TCAS-1'23 [3]	TCAS-II'20 [4]	ISSCC 17 [5]	VLSI 16 [6]	ISSCC 18 [7]	VLSI 20 [8]
Algorithm	DL	BD-NS-EPA	EP-wNSA	MMSE	CHEMP	EPD	DCD
MIMO (N _r , N _t)	128×32	128×32	128×32	128×8	128×32	128×16	256×32
Mod. (QAM)	4-256	64	4-256	256	256	4-256	4-256
Channel adaptiveness ¹	yes	yes	yes	no	no	yes	yes
Link margin gain [dB] ²	4.3	3.7	3.7	0.0	Error floor	4.3	0.7
Result type	Fabricated	Layout	Layout	Fabricated	Fabricated	Fabricated	Fabricated
Voltage [V]	1.05	1.0	1.0	0.9	0.9	1.0	1.1
Tech. [nm]	28	65	65	28	40	28	40
Area [mm ²]	6.25	2.91	2.65	1.1	0.58	2.0	0.73
Freq. [MHz]	217	500	500	300	425	569	290
Power [mW]	459	571	955	18	221	127	87
T/P [Gb/s]	5.76	0.72	0.86	0.30	2.76	1.80	1.96
Energy Eff. [pJ/b]	79.7	793.1	1110.5	60.0	80.1	70.6	44.4