IDEC Chip Design Contest

Transposable eDRAM-based Computing-In-Memory System for SNN On-chip Unsupervised Learning

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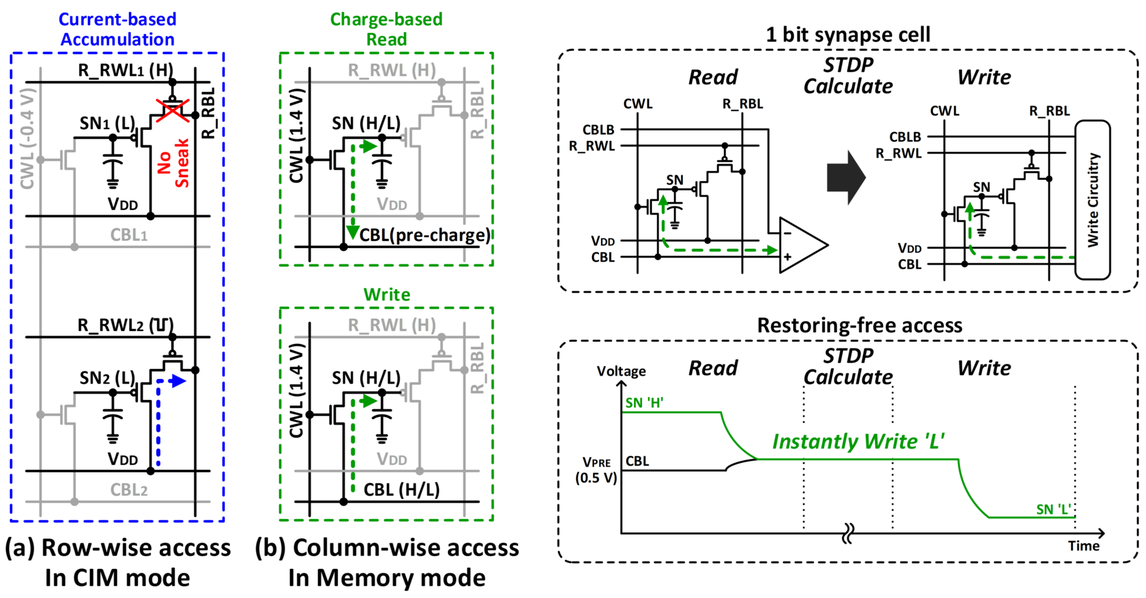
Introduction

- **Low Area Efficiency of Transposable CIM Bitcells**
  - SRAM requires a minimum of two extra transistors for transposable memory implementation for on-chip learning.
  - MRAM/ReRAM-based CIMs provide high memory density but are not compatible with standard CMOS process.
- **Two challenges of eDRAM-based CIM Bitcells**
  - Sneak current through unselected cells degrade both power efficiency and sensing margin.
  - Charge sharing-based sensing incurs energy overhead due to the required write-back operation after destructive read.
- **Challenge of ADC integration in Analog CIMs**
  - Analog CIMs require high-resolution ADCs, resulting in significant energy overhead.

Transposable 3T1C eDRAM Cell

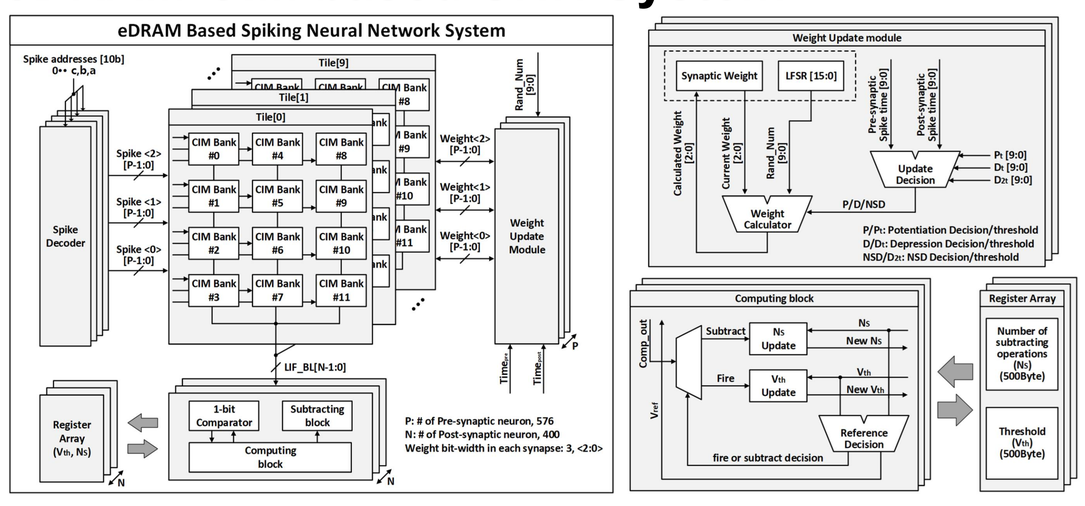
- **The proposed eDRAM Bitcell**
  - In row-wise access, the three-transistor structure prevents the formation of sneak current paths.
  - In column-wise access, the read-calculate-write sequence enables restoring-free access.



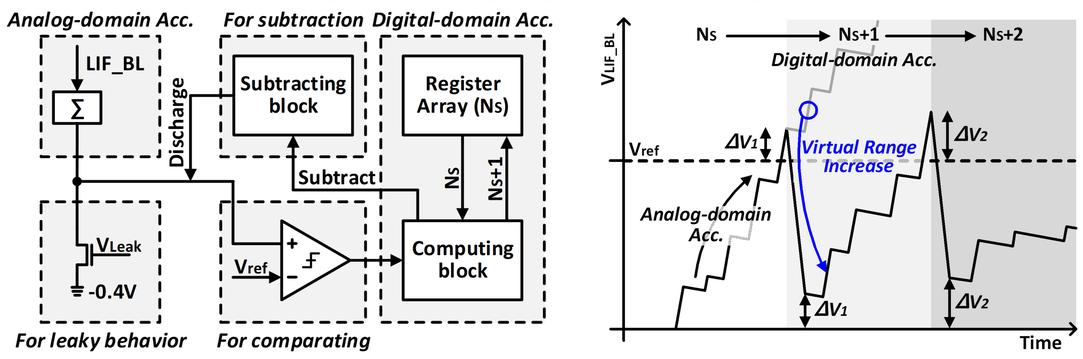
- **The proposed Dual-mode Sense Amplifier**
  - Offset cancellation is required due to the inherently low read margin of charge sharing mechanism in logic process.
  - The proposed sense amplifier supports two modes: refresh and restoring-free access mode.
  - Leveraging this sense amplifier improves learning energy efficiency by up to 27%.

The proposed SNN Accelerator

- **eDRAM-CIM based SNN System**

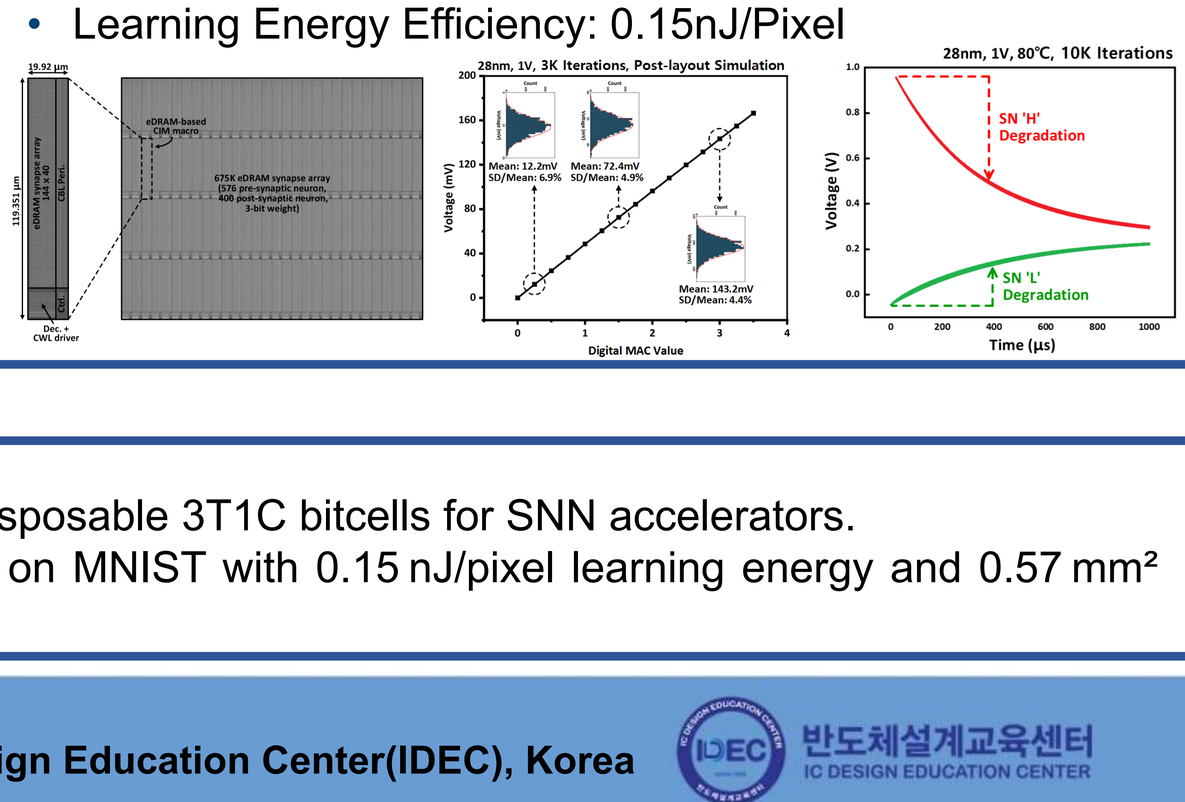


- **Mixed Signal based Neuron model**
  - It enhances signal integrity and energy efficiency.



Results

- System Area: 0.57mm^2 (675 kb Synapse Array)
- CIM Macro Area: 2377 μm² (119.351 μm × 19.92 μm)
- Synapse Array: 5.76 kb (144 × 40)
- Voltage Deviation of LIF_BL: σ ≈ 5.08% of mean voltage
- Retention Time: 120 μs refresh cycle
- Learning Energy Efficiency: 0.15nJ/Pixel



Conclusion

- We present a novel eDRAM-based CIM architecture with transposable 3T1C bitcells for SNN accelerators.
- The implemented SNN processor achieves 89.6% accuracy on MNIST with 0.15 nJ/pixel learning energy and 0.57 mm² area in a 28 nm CMOS process.

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