IDEC Chip Design Contest

Precharge-Controlled 4T1C eDRAM Macro for Reconfigurable Digital Compute-in-Memory with Dual Multiplication Modes

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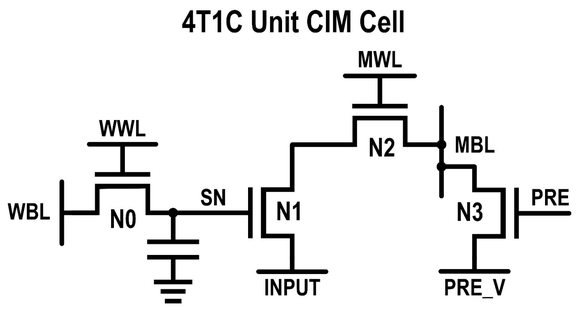
Introduction

- Edge AI demands energy-efficient and reconfigurable CIM architectures.
- Conventional CIM lacks adaptability due to fixed bit-widths and restricted logic operations.
- To overcome these limitations, we propose a precharge-controlled 4T1C eDRAM-based DCIM macro with dual-mode (AND/XNOR) multiplication and reconfigurable INT1-8 MAC operations.



AND Operation

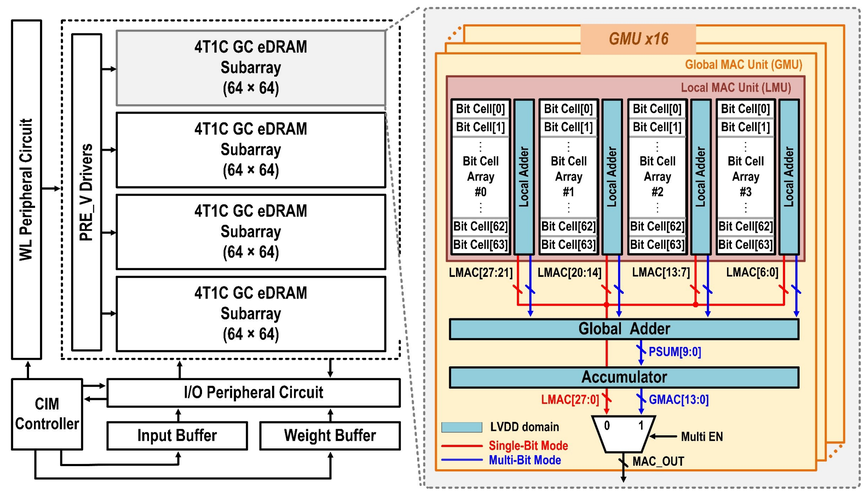
SN	INPUT	MBL (Precharge)	MBL (AND Result)
0	0	0	0
0	VDD	0	0
VDD	0	0	0
VDD	VDD	0	VDD-V_{TH}

XNOR Operation

SN	INPUT	MBL (Precharge)	MBL (XNOR Result)
0	0	VDD	VDD
0	VDD	0	0
VDD	0	VDD	0
VDD	VDD	0	VDD-V_{TH}

Overall Architecture

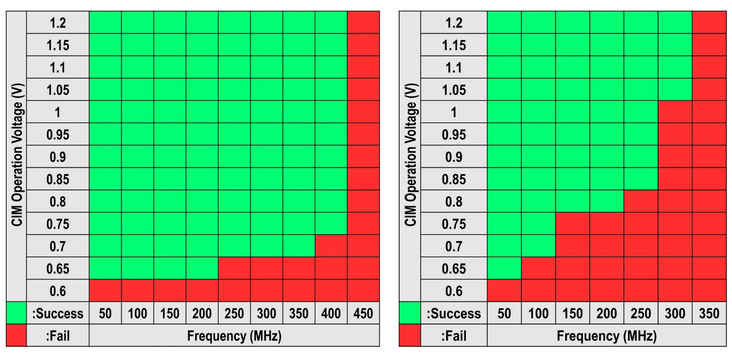
- The proposed 4T1C eDRAM cell supports both AND and XNOR operations through precharge control, enabling dual-mode multiplication in a single cell.
- A custom MOMCAP enhances data retention without increasing cell area.
- The 16Kb macro performs efficient MAC operations using bit-serial processing and shared adder structures.
- A 15:4 area-efficient adder reduces logic overhead and supports signed/unsigned multi-bit operations.



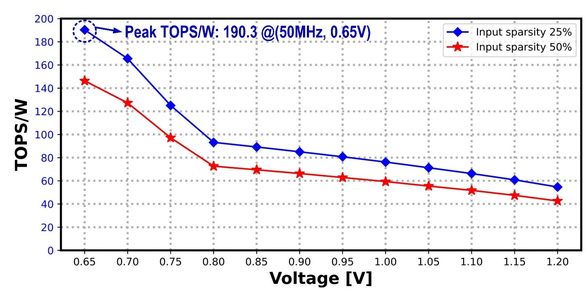
<Overall architecture of 4T1C eDRAM>

Measurement Results

- CIM functionality was validated using an FPGA-based setup over 0.65-1.2V.
- Shmoo plots confirmed stable 1b-1b and 4b-4b MAC operations, with reduced margins in 4b-4b due to the use of global adder and accumulator.



<Shmoo plot, L: 1b-1b, R: 4b-4b>



<Supply voltage for 4b-4b>

Conclusion & Acknowledgement

- The proposed DMM-DCIM macro achieved 190.3 TOPS/W and 28.9 TOPS/mm^2 in 4b-4b operations.
- CIM operations were verified up to 400MHz (1b-1b, >0.7V) and 300MHz (4b-4b, ≥1.05V)
- These results demonstrate that the proposed structure is an efficient CIM solution for edge AI applications.
- The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

< Performance summary >

Process	28 nm CMOS
Memory Type	eDRAM
Array Size	16Kb
Cell Structure	4T1C
DRT	57.4-211
Dual Multiply	XNOR/AND
Energy Efficiency (TOPS/W)	517.6(1b-1b) 190.3 (4b-4b)
Area Efficiency (TOPS/mm^2)	873.8(1b-1b) 28.9 (4b-4b)

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