IDEC Chip Design Contest

DLO-DCIM: A Dual-Logical-Operation 9T-SRAM-Based Digital Compute-In-Memory Macro Supporting Independent Bit Line Control-Based Dual Row Access

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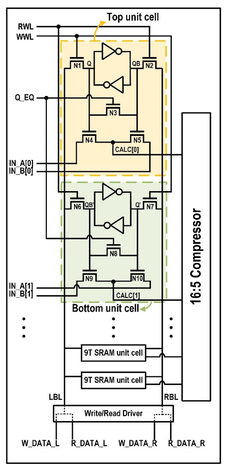
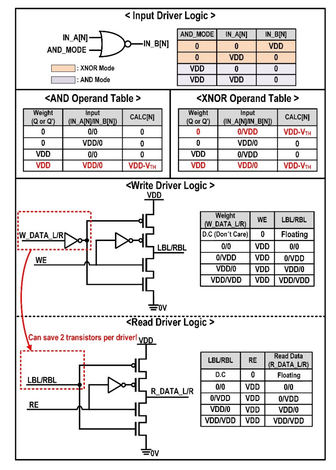
Introduction

- CIM overcomes von Neumann bottlenecks in AI and edge computing.
- Digital CIM improves accuracy and parallelism, but energy and area efficiency are still key for edge use.
- This work introduces a 9T SRAM-based DLO-DCIM macro that supports both XNOR and AND operations, with bit-level reconfigurability and dual-row access enabled by independent bit-line control.



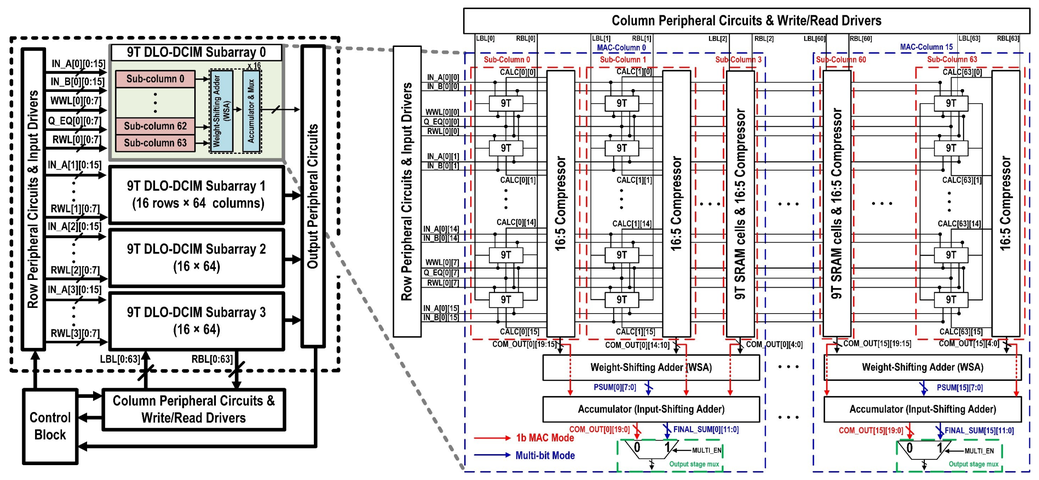
<Circuit diagram of 9T SRAM>



<Operand table>

Overall Architecture

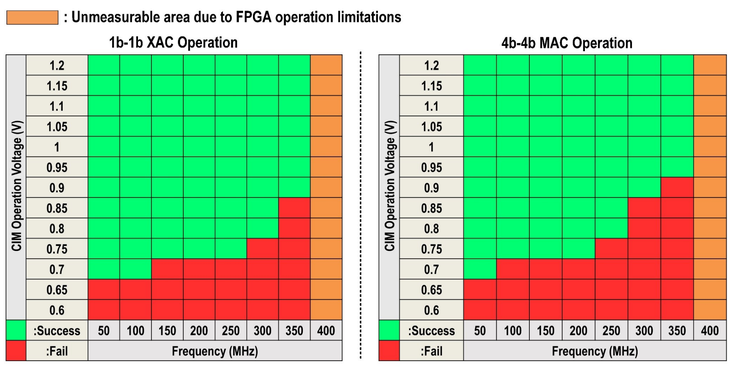
- The DLO-DCIM supports both XNOR and AND operations within each 9T SRAM cell by combining input-driven logic with embedded memory storage.
- The IBLC-DRA scheme enables efficient dual-row access with zigzag-configured access transistors, achieving 100% full-precision operation without cell redundancy.
- A reconfigurable adder structure supports multiple precisions and significantly reduces transistor count.
- The Q_EQ pulse equalizes internal storage nodes during write, enhancing stability in single-ended operations under PVT variation.



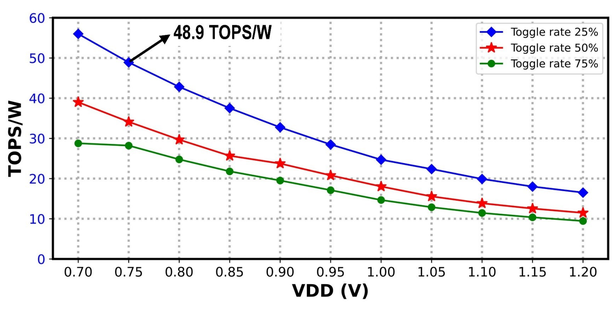
<Overall architecture of 9T SRAM>

Measurement Results

- CIM functionality was validated using an FPGA-based setup across 0.7-1.2V.
- Shmoo plots confirmed stable 1b-1b and 4b-4b MAC operations, with reduced margins in 4b-4b due to the use of a global adder and accumulator.



<Shmoo plot, L: 1b-1b, R: 4b-4b>



<TOPS/W for 4b-4b>

Conclusion & Acknowledgement

- The proposed 4-Kb DLO-DCIM macro achieved 48.9 TOPS/W and 3.58 TOPS/mm² during 4b-4b MAC operation at 0.75 V and 200 MHz.
- CIM operations were verified up to 350 MHz (1b-1b, ≥ 0.9V) and 350 MHz (4b-4b, ≥ 0.95V)
- These results validate the proposed architecture for edge AI with energy and area constraints.
- The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

< Performance summary >

Process	28 nm CMOS
Memory Type / Cell Structure	SRAM / 9T
MAC Method / Macro Capacity	Digital / 4Kb
[a] Norm. Row Access Number	8
Various Multiply Mode	XNOR/AND
Energy Efficiency (TOPS/W)	593.5 (1b-1b) 48.9 (4b-4b)
Area Efficiency ($TOPS/mm^2$)	95.57 (1b-1b) 3.58 (4b-4b)

[a]: # of row access × 1Kb / macro capacity