IDEC Chip Design Contest

An NRZ Transceiver for Low-Power Memory Interfaces Achieving 13 Gbps at 0.52 pJ/bit Transmitter and 12 Gbps at 0.073 pJ/bit Receiver.

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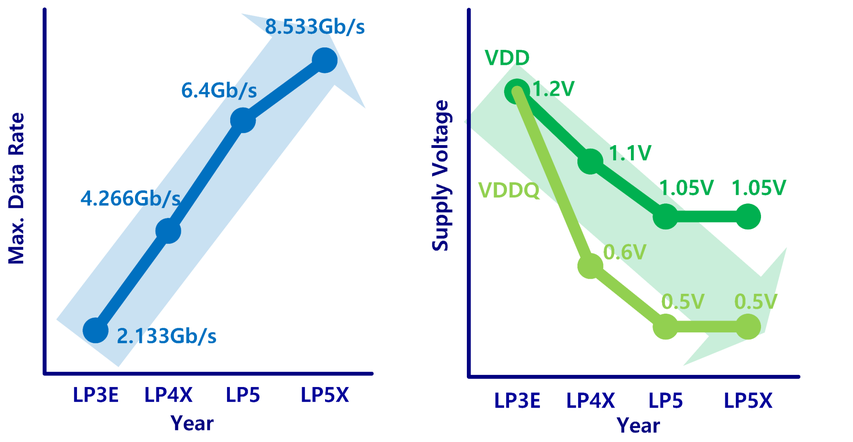
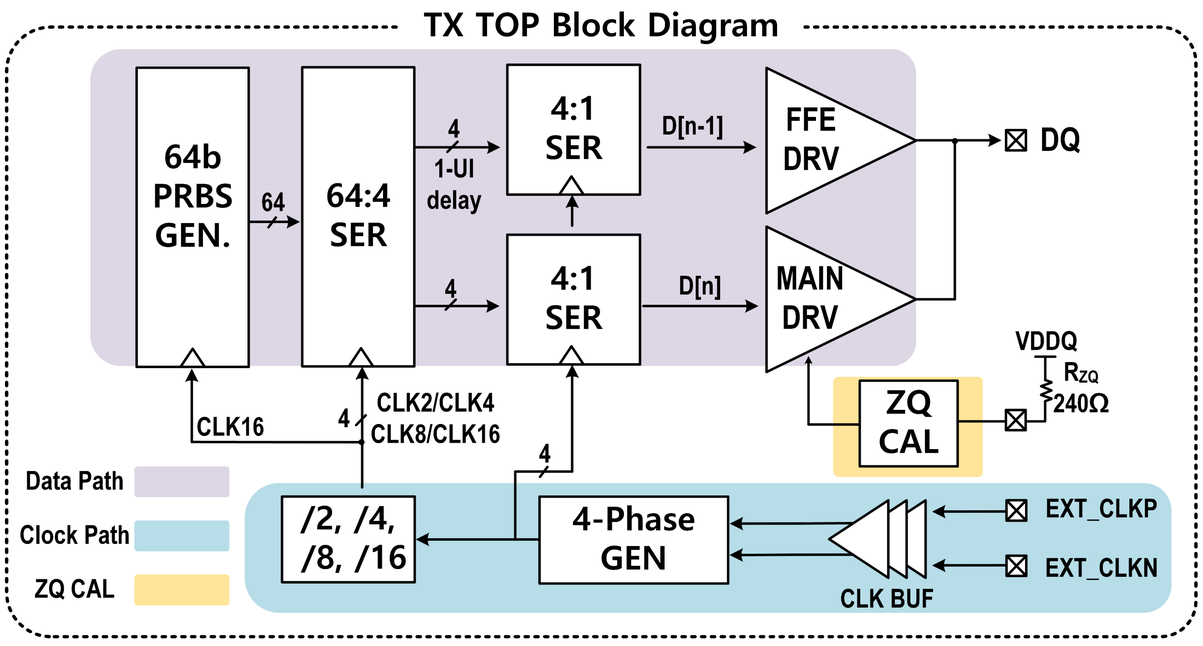
Introduction

- The next-generation LPDDR memory is being developed to achieve higher data rates while operating at even lower supply voltages.
- Multilevel signaling, such as PAM, suffers from reduced SNR, which becomes more critical at low supply voltages.
- The proposed TRX uses NRZ signaling for low supply voltage and a quarter-rate clock to enhance timing margin.

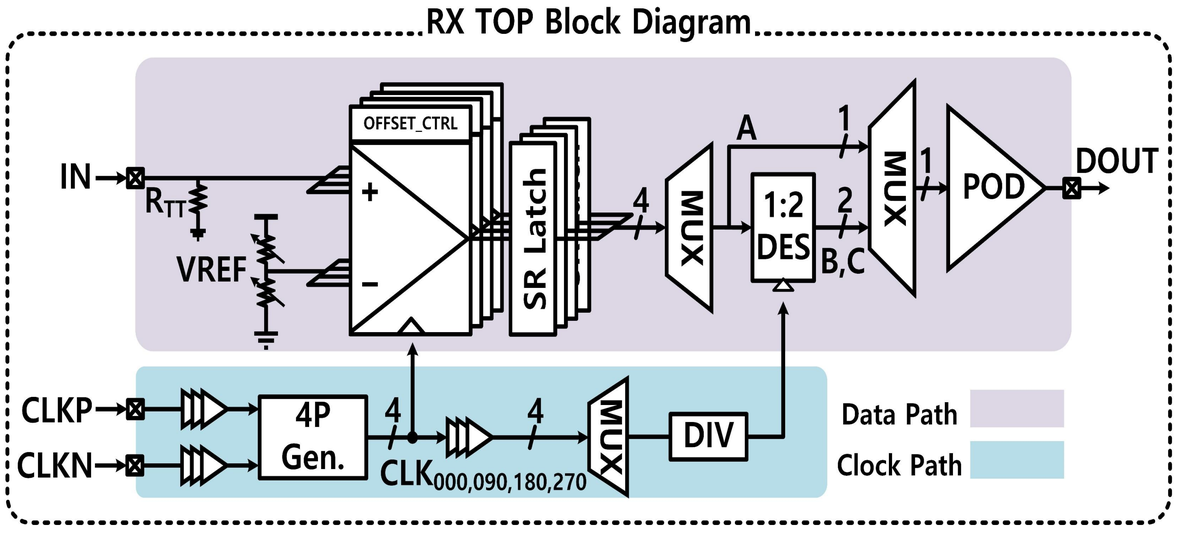


TX Implementation



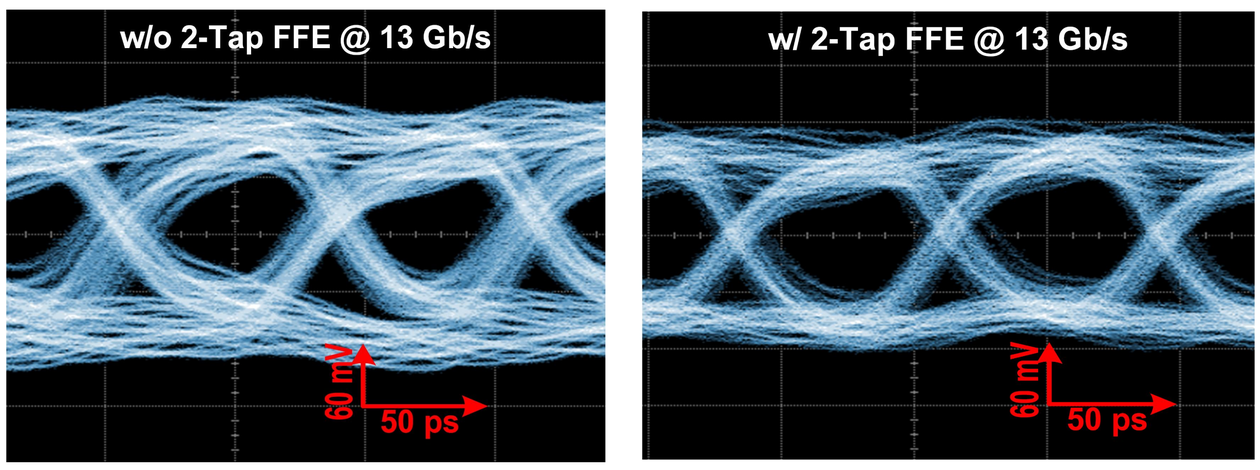
- The proposed architecture utilizes a 2-tap FFE driver with de-emphasis to compensate channel ISI.
- A ZQ calibration is implemented for impedance matching.

RX Implementation



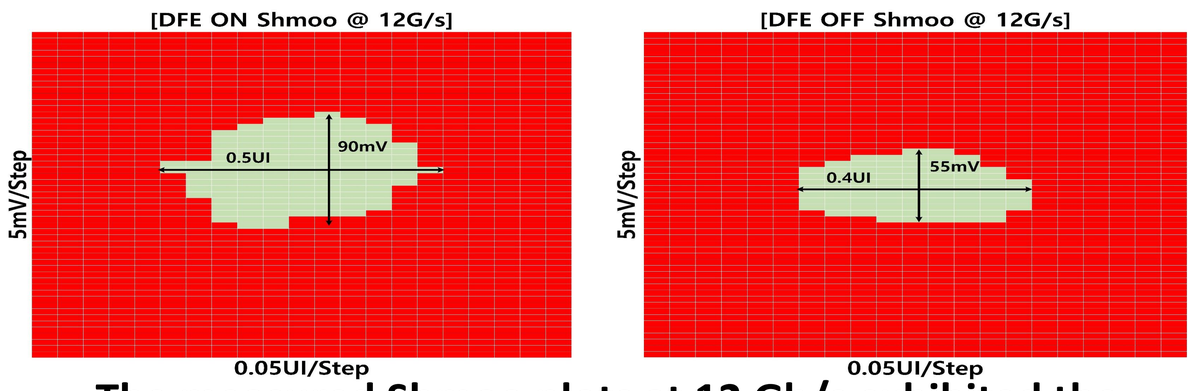
- A 1-tap DFE is used to compensate for ISI.
- The proposed architecture performs 2-bit offset calibration to compensate for input offset.
- A 1:2 deserializer is implemented for high-speed serial-to-parallel data conversion.

TX Measurement Result



- The measured eye diagrams at 13 Gb/s showed an opening width of 48.2 ps and a height of 81.1 mV , achieving 0.52pJ/bit.

RX Measurement Result



- The measured Shmoo plots at 12 Gb/s exhibited the effectiveness of the 1-tap DFE.
- With DFE enabled, the RX achieved a timing margin of 0.5UI and a voltage margin of 90mV, achieving 0.073pJ/bit.

Conclusion and Acknowledgement

- Our proposed TRX surpasses the speed of LPDDR5X defined in the JEDEC specification while achieving low power efficiency using NRZ signaling.

- The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.