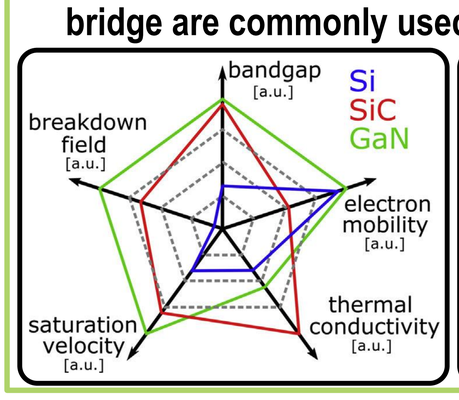
IDEC Chip Design Contest

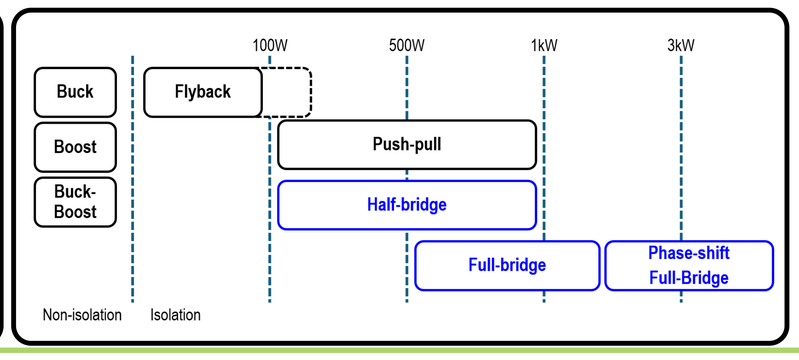
A High-Voltage Gate Driver IC with High CMTI and Integrated SPI Trimming

Myeong-Ho Kim and Se-Un Shin
Pohang University of Science and Technology (POSTECH), Korea

1. Introduction

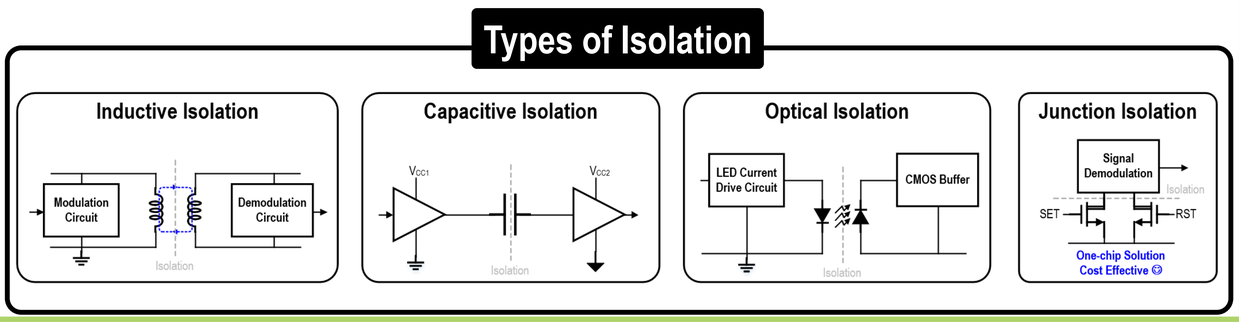
- WBG semiconductors offer superior performance compared to Si, enabling much faster switching speeds than conventional Si-based MOSFETs or IGBTs.
- However, due to their distinct characteristics, WBG devices require specialized gate drivers.
- In high-power applications, circuit topologies such as half-bridge or full-bridge are commonly used.





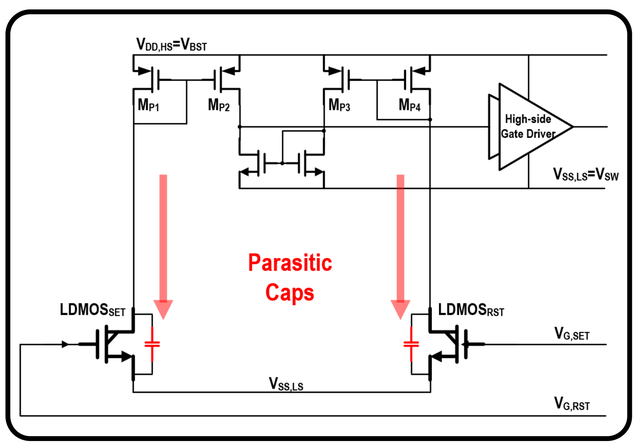
- To drive high-side switches, signal isolation is required due to the different voltage domain between the controller and the power stage.
- Various isolation techniques are used, including inductive isolation using magnetic coupling, capacitive isolation using electric coupling, optical isolation using optocouplers, and junction isolation using LDOMSs.
- Among these, junction isolation stands out as it can be implemented on a single chip, offering significant cost advantages over other approaches.

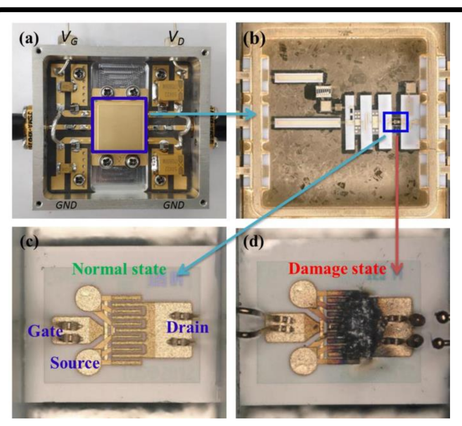
Types of Isolation



2. Issues

- When a signal to turn on the high-side switch is received, a pulse voltage is applied to the gate of the HV LDMOS, generating a pulse current through the left branch of the level shifter.
- This pulse signal is transferred to the high-voltage domain and demodulated, thereby turning on the high-side switch.
- Once the high-side switch is turned on, a large voltage transition (dv/dt) occurs at the V_{SW} node.
- ☹ Due to the large parasitic capacitance of the HV LDMOS, substantial current flows through both branches, causing false triggering. This can lead to malfunction of the converter and damage to the device.



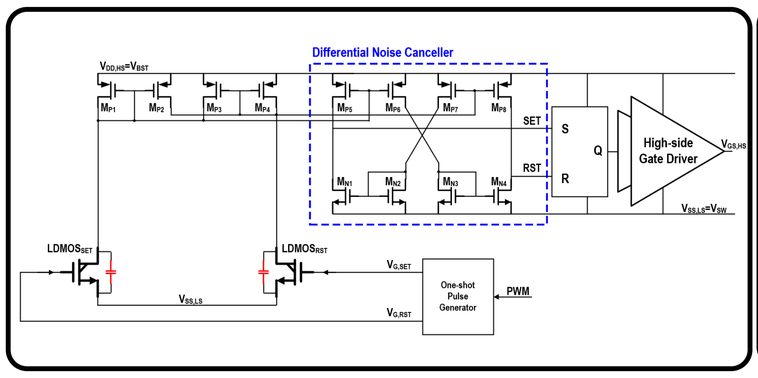


Zhao, J., Zhao, G., Chen, Q. et al. Damage effects in GaN high electron mobility transistor power amplifier induced by high power microwave pulses. Sci Rep 15, 5988 (2025). https://doi.org/10.1038/s41598-025-89938-6

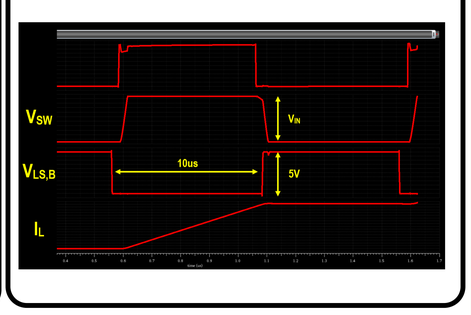
- The characteristics of fabricated chips often differ from the original design.
- To compensate for these variations, we include externally controllable trimming pins for post-fabrication adjustment.
- ☹ However, implementing many trimming options requires many trimming pads, which leads to increased chip area.

3. Proposed Work

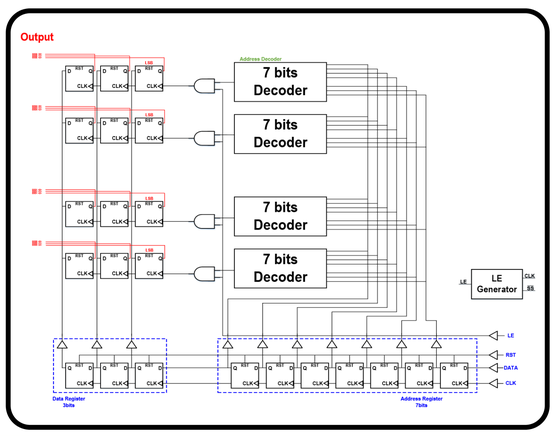
- The current generated by the combination of the dv/dt component and the parasitic capacitance of the HV LDMOS is ideally balanced through a symmetric layout, resulting in equal current flow.
- This current is then canceled by the current mirror structure in the subsequent differential noise canceller circuit, thereby improving CMTI (Common Mode Transient Immunity).



Simulation Result



- SPI (Serial Peripheral Interface) is a standard protocol for communication between a chip and external devices.
- In this design, a reconfigurable full-custom SPI circuit is implemented, enabling communication with the external system using only four pads.
- The trimming signals are stored in an internal shift register and utilized for flexible trimming control within the chip.



Simulation Result

5. Conclusion

- This work improves the noise Immunity (CMTI) performance of conventional level shifter structures by incorporating a differential noise canceller circuit.
- In addition, a reconfigurable full-custom SPI circuit is implemented for trimming, effectively reducing the number of pads required.

<Acknowledgement>
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