IDEC Chip Design Contest

Guard Ring Optimization for CMOS SPADs in 28 nm RF Technology

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[Introduction]

- Application: SPADs are essential in ToF sensing and biomedical imaging due to its high sensitivity.
- Requirement: Miniaturization is critical for high-resolution sensor integration.
- Challenge: 28 nm RF CMOS enables scaling but increases DCR due to high doping concentrations.
- Goal: Optimization for low DCR and high fill factor, achieving both compactness and performance.

[Body]

(1) Concept & Background

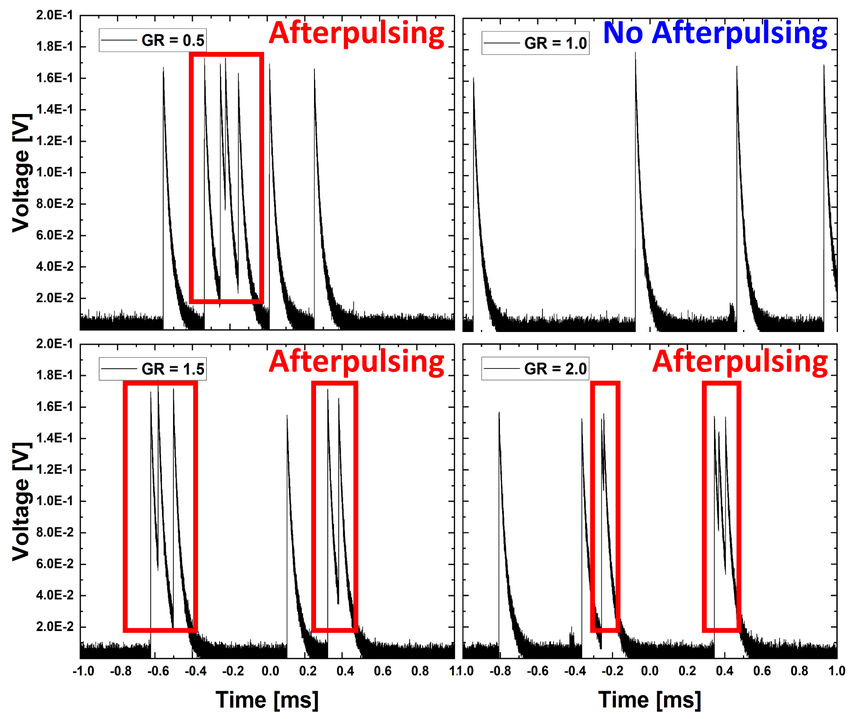
- Guard ring (GR): commonly implemented for edge breakdown prevention.
- Constraint: Only STI-based guard rings are allowed due to design rules.
- Issue: STI can act as a noise source → dark count rate (DCR) increased.
- Goal: Identify an optimized guard ring width that minimizes DCR while improving fill factor.

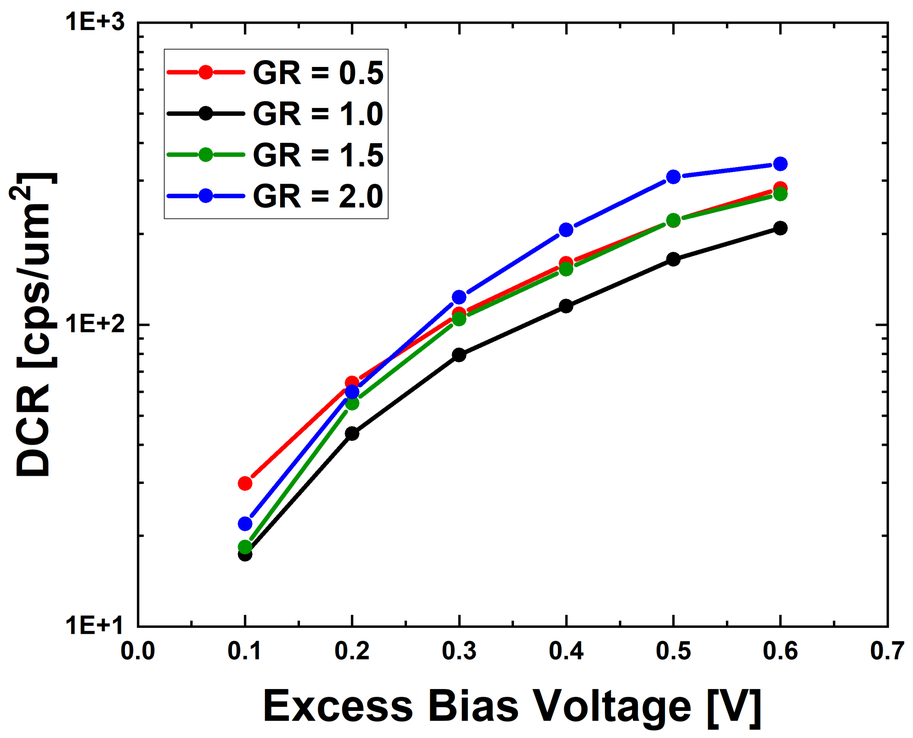
(2) Design & Fabrication

- SPADs designed with four guard ring widths: 0.5 µm, 1 µm, 1.5 µm, 2 µm.
- Active area and core structure kept identical for fair comparison.

(3) Measurement Results

- DCR:
  - Lowest DCR at 1 µm guard ring
  - High DCR at 0.5 µm due to strong electric field (short distance between anode and cathode)
  - Increased DCR at ≥ 1.5 µm due to larger STI area (expanded STI area acts as a stronger noise source)





- Fill Factor:
  - 1 µm GR structure: 1.2× higher FF than 1.5 µm GR structure, 1.5× higher than 2 µm GR structure.

(4) Limitation & Improvement Plan

- Limitation: STI guard ring between anode and cathode introduces DCR.
- Solution: Auto-generation of N+ and PW layer should be replaced to designed layer of N+ and PW, allowing guard ring structures other than STI guard ring.

[Conclusion]

- 1 um guard ring design shows optimal trade-off between DCR and fill factor.
- Guard ring optimization enables both SPAD miniaturization and performance enhancement.