IDEC Chip Design Contest

2025 IDEC Congress CDC

A 1.12-ps Resolution Flash ADC-Assisted Coarse-to-Fine Time-to-Digital Converter with ADC Reference Voltage Calibration and Digital Linearity Correction

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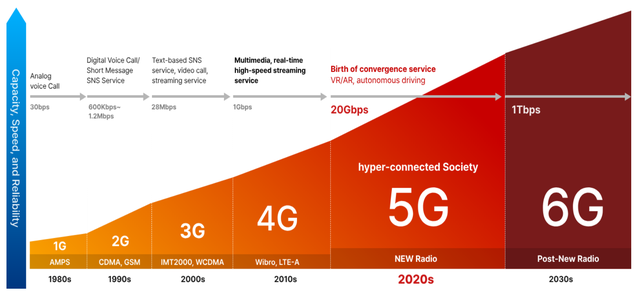
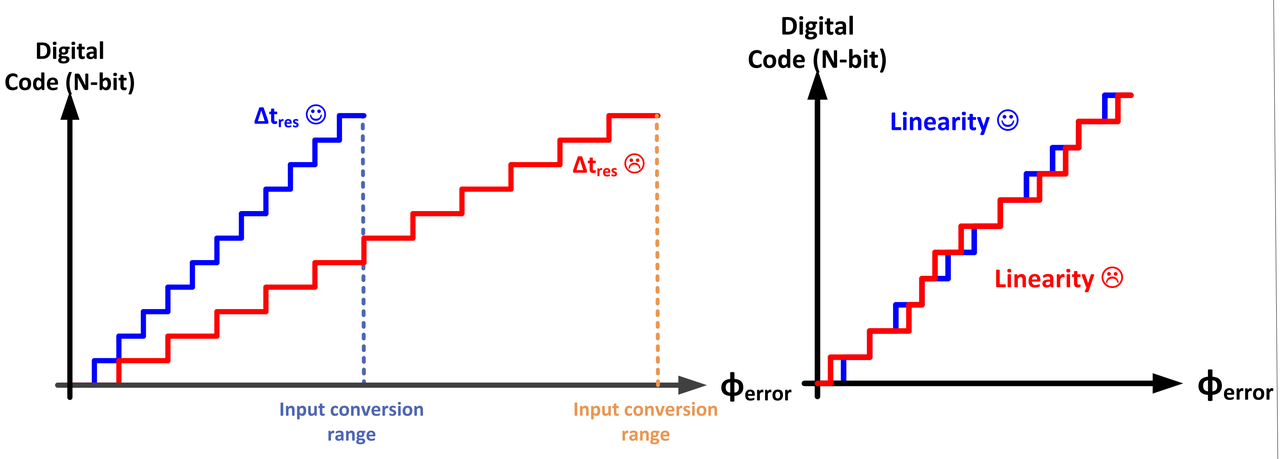
Introduction



TDCs are essential for high-speed systems that require fine time resolution

High-resolution TDC designed with:

- **Wide measurement range**
- **High linearity**
- **ADC-assisted architecture**



Linearity Improvement Technique

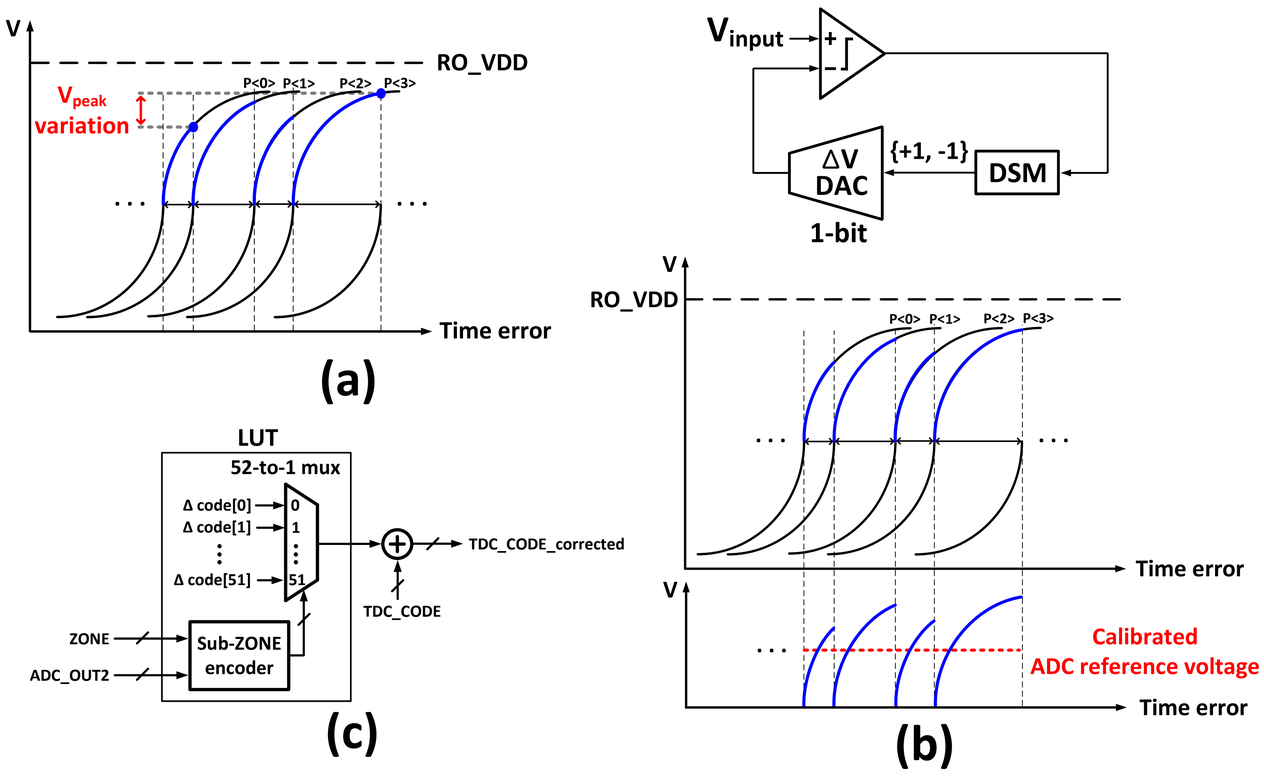


Figure 3. (a) ADC input voltage variation caused by non-uniform phase spacing, (b) ADC reference voltage calibration, (c) TDC linearity correction

System Architecture

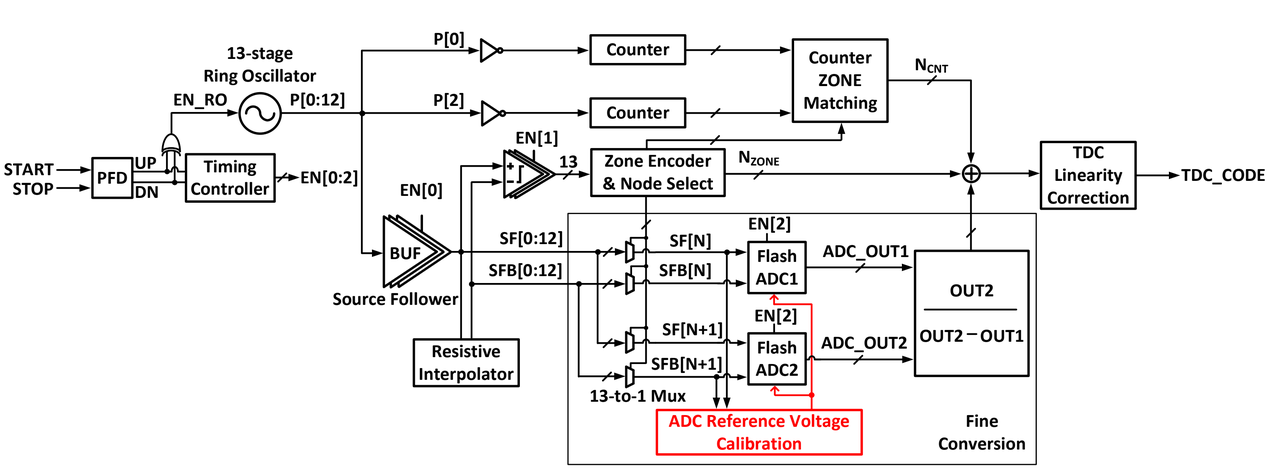


Figure 1. Block diagram of the proposed TDC

The proposed TDC employs:

- **Ring-oscillator-based coarse-to-fine TDC**
- **Coarse conversion: multi-phase encoding**
- **Fine conversion: ADC-based voltage ratio measurement**

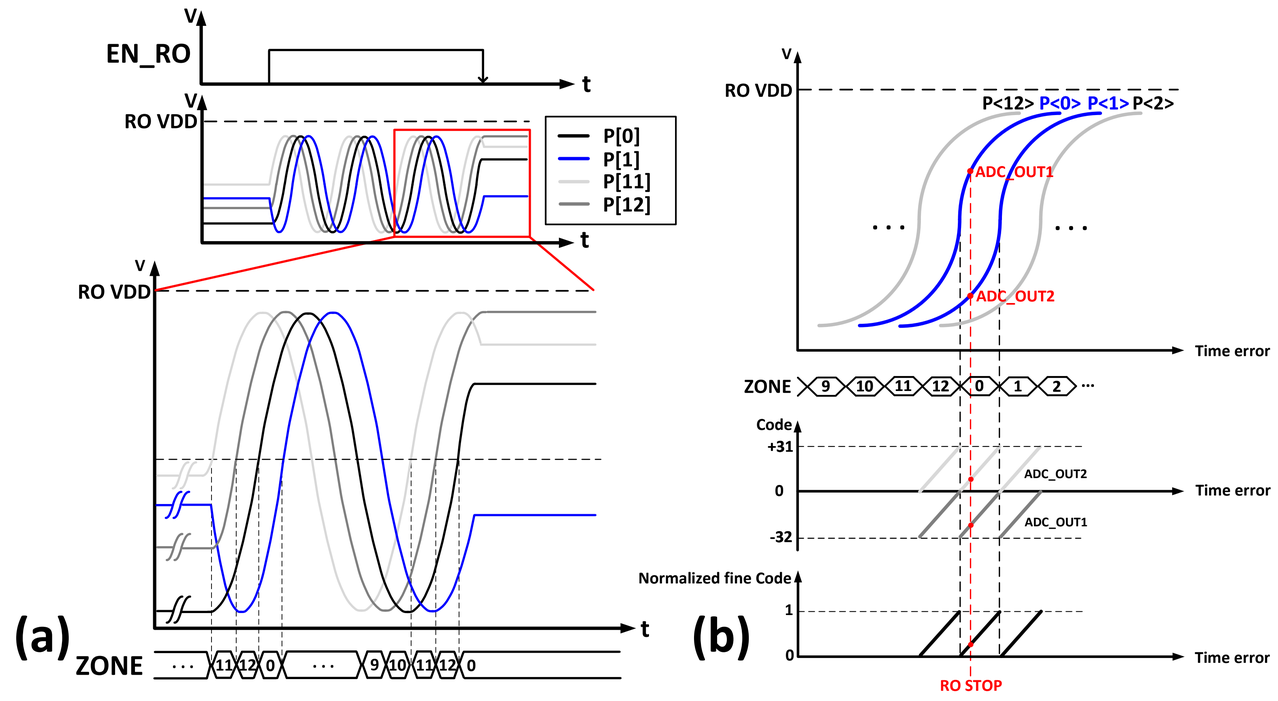


Figure 2. TDC conversion process: (a) coarse conversion, (b) fine conversion

Conclusion

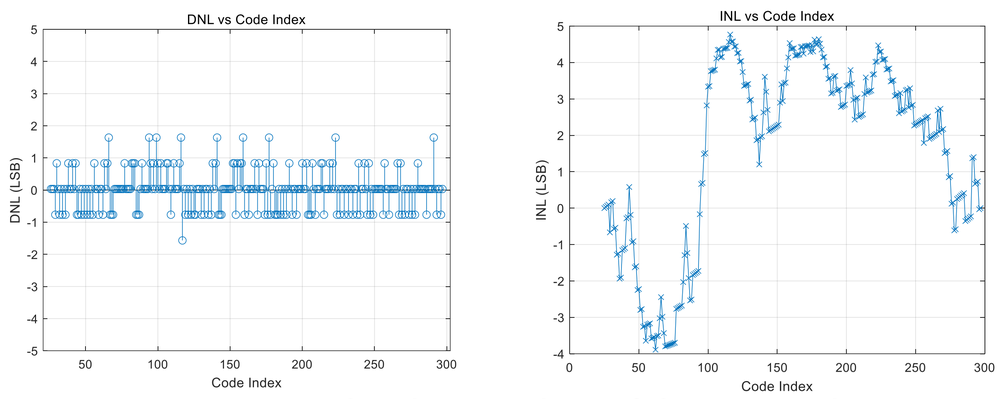


Figure 4. Simulated DNL and INL of the proposed TDC

- **Achieves 1.12-ps resolution using an ADC-assisted coarse-to-fine architecture**
- **Supports 63-ns input dynamic range with an 8-bit counter in a ring-oscillator-based TDC**
- **Enables 5.6-ns conversion time by employing a flash ADC for fine conversion**
- **Linearity improvement by applying:**

1. **ADC reference voltage calibration (DNL 10 LSB -> 3.8 LSB)**
2. **Digital linearity correction (DNL 3.8 LSB -> 1.6 LSB)**

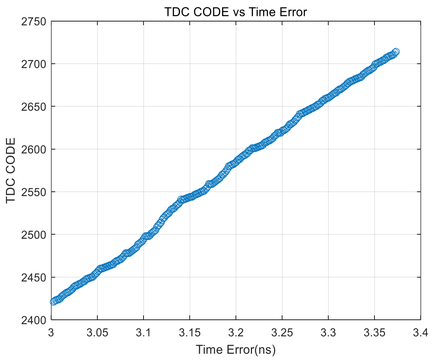


Figure 5. Time error vs TDC CODE

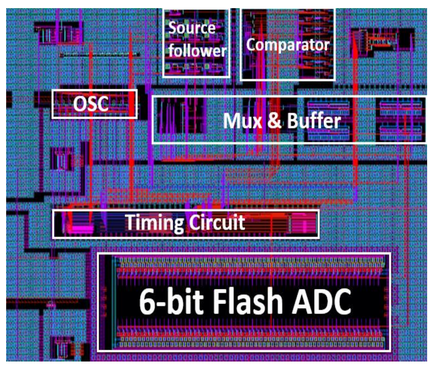


Figure 6. Layout view

	JSSC 12 Y.H Seo	JSSC 13 J.S. Kim	JSSC 14 K.S. Kim	This Work
Resolution	1.25ps	1.76ps	1.12ps	**1.12ps**
Input dynamic range	1.25ns	1.80ns	588ps	**63ns**
Conversion time	10ns	3.33ns	100ns	**5.6ns**
DNL	± 0.7 LSB	± 0.6 LSB	± 0.6 LSB	**± 1.5 LSB**
INL	± 3 LSB	± 1.9 LSB	± 1.7 LSB	**± 5 LSB**
Area	0.07mm^2	-	0.14mm^2	**0.645mm^2**
Power	4.3mW	115mW	15.4mW	**5.42mW**
Process	130nm	130nm	65nm	**28nm**

Table 1. Performance comparison