IDEC Chip Design Contest

A D-Band Frequency Doubler based on 28-nm CMOS Technology

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Introduction

Amplifier-frequency-multiplier chain (AMC) is widely adopted for implementing a terahertz source. AMCs can implement relatively wideband sources, making them more suitable for achieving high-resolution radar systems [1]. In this work, a D-band frequency doubler is designed as a part of signal source based on 28-nm CMOS technology.

1. Circuit Design

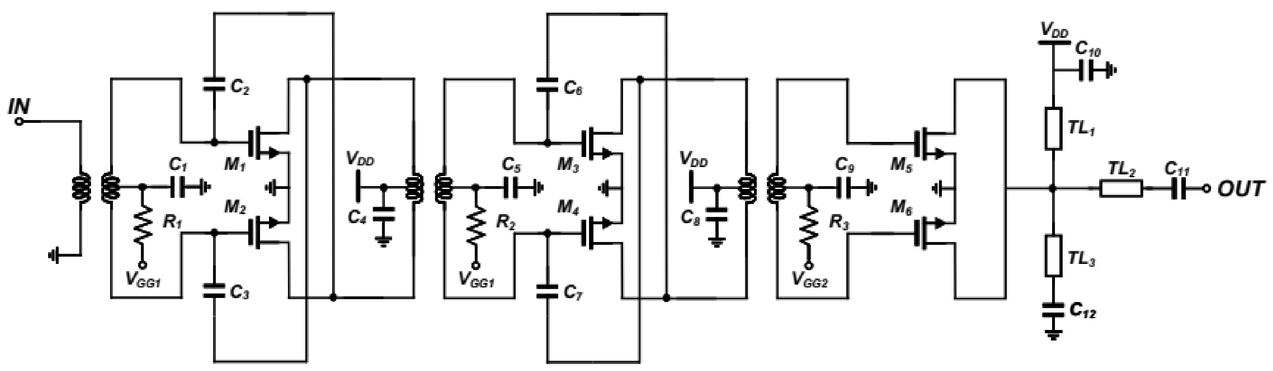

Fig. 1. Schematic of the frequency doubler.

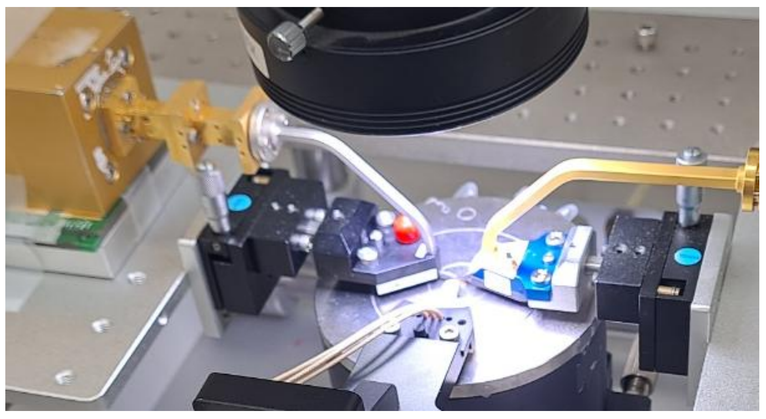

Fig. 3. Measurements setup

- Fig. 1 shows the schematic of the frequency doubler.
- A 2-stage common-source amplifier topology was adopted for the 70-GHz drive amplifier, which employs the capacitive neutralization (C_2,C_3 ,C_6 ,C_7).
- The capacitive neutralization technique is adopted to improve stability and gain [2].
- The interstage matching networks were implemented with transformers which achieve the conjugate matching between each stage.
- The common-source push-push structure employed for doubler.

2. Simulation Result

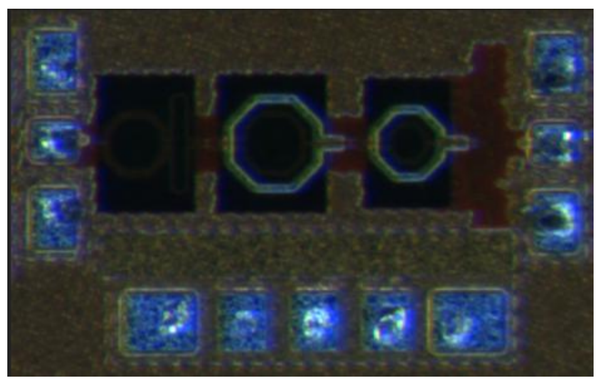

Fig. 2. Chip photo.

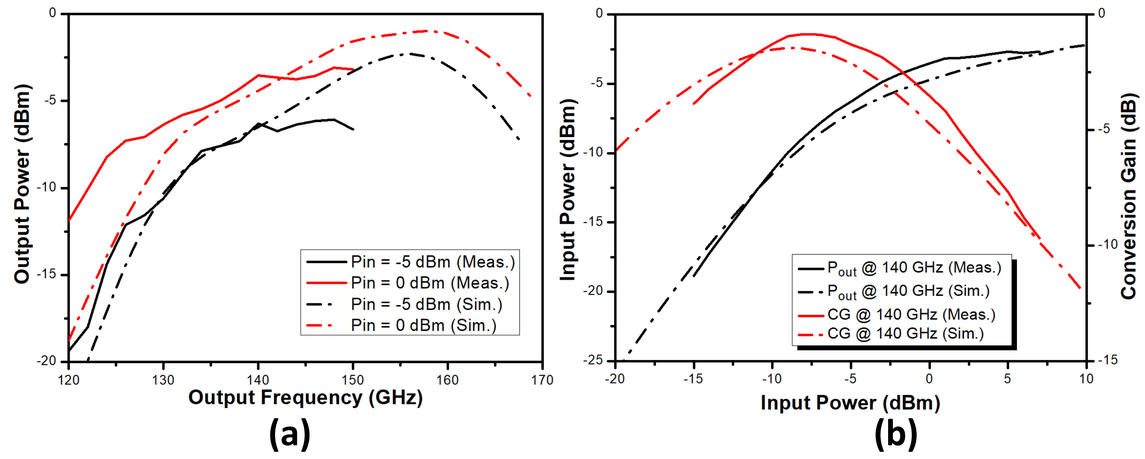

Fig. 4. Simulated results of frequency doubler.

- Fig. 2 shows the chip photo of the fabricated frequency doubler.
- The chip size is 528 × 873 μm^2 including pads.
- The measurements setup of the frequency doubler is shown in Fig. 4.
- In Fig. 3(a), the peak output power is -3.09 dBm at 148 GHz with input power of 0 dBm. The 3-dB bandwidth with input power of 0 dBm is 18 GHz, ranging from 132 GHz to 150 GHz.
- In Fig. 3(b), the saturated output power is -3.5 dBm at 140 GHz with input power of 0 dBm.

Conclusion

A D-band frequency doubler has been designed in this work based on 28-nm CMOS technology. It has peak output power of -3.09 dBm at 148 GHz with 0 dBm input power and saturated output power of -3.5 dBm at 140 GHz with input power of 0 dBm. This circuit will be measured with spectrum analyzer and power meter to evaluate output frequency and output power. The designed frequency doubler can be applied to D-band LO signal generator for wireless communication or radar system.

Acknowledgement

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Reference

[1] J.-S. Rieh and SpringerLink, *Introduction to Terahertz Electronics*, 1st 2021. ed. Cham: Springer International Publishing : Imprint: Springer (in English), 2021.

[2] H. Asada, K. Matsushita, K. Bunsen, K. Okada, and A. Matsuzawa, "A 60 GHz CMOS Power Amplifier Using Capacitive Cross-Coupling Neutralization with 16% PAE," (in English), *Eur Microw Conf*, pp. 1115-1118, 2011. [Online]. Available: <Go to ISI>://WOS:000411595800282.