IDEC Chip Design Contest

Implementation of Area-Efficient DRAM Sense Amplifier

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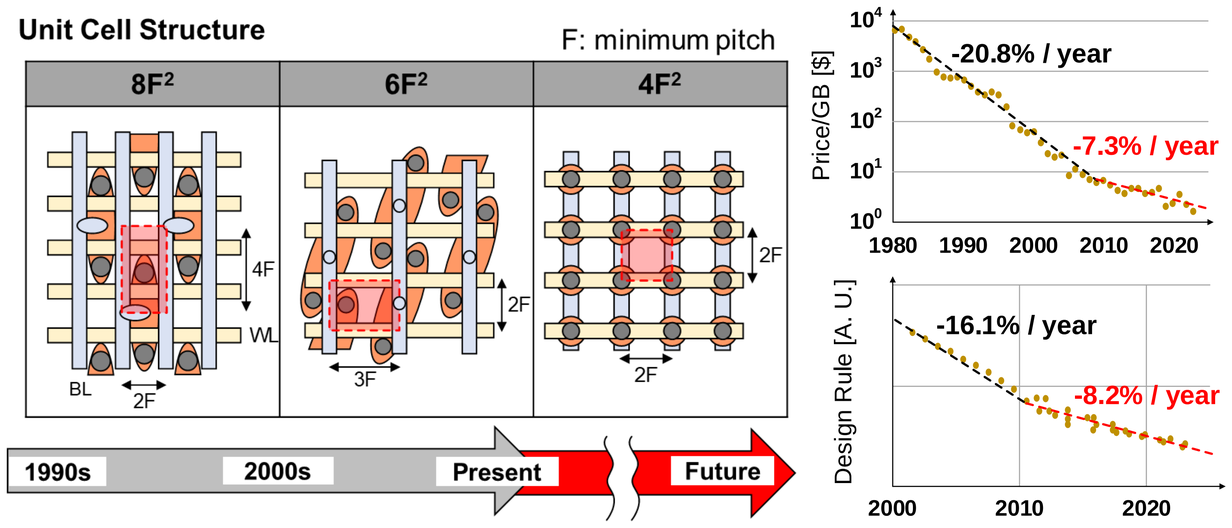
Introduction

Challenges of DRAM Density Scaling

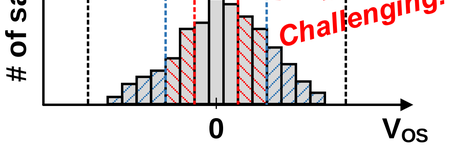
- Saturation on cell structure, design rule and price.

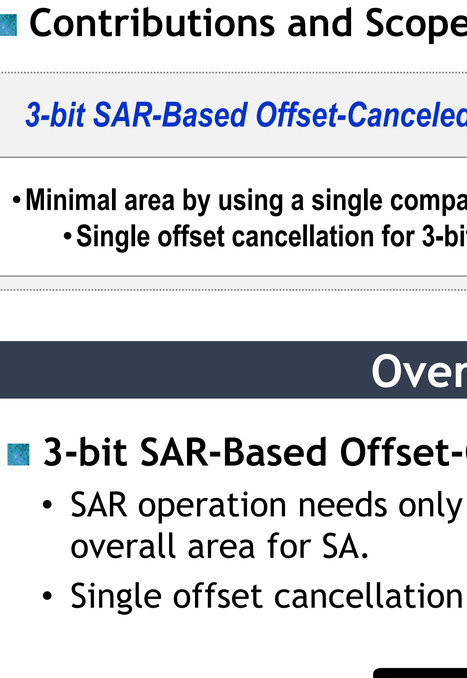


Challenges of Multi-Bit Sense Amplifier

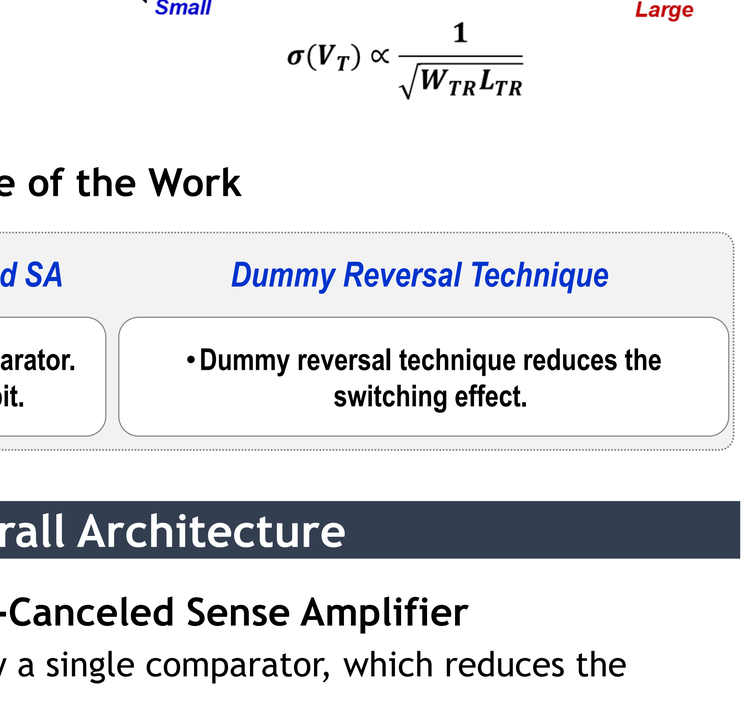
- Multi-bit cell can reduce the overall area but requires higher performance specification for sense amplifier(SA).

Mismatch of SA Offset





Trade-Off between Mismatch and Area



$$\sigma(V_T) \propto \frac{1}{\sqrt{W_{TR}L_{TR}}}$$

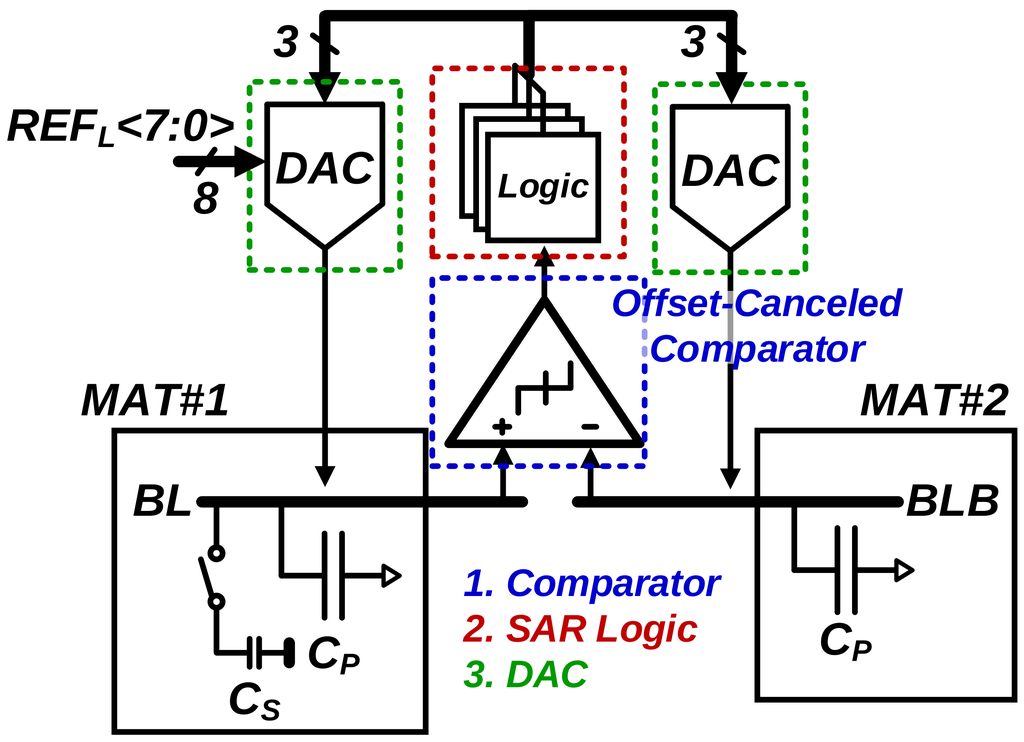
Contributions and Scope of the Work

3-bit SAR-Based Offset-Canceled SA	*Dummy Reversal Technique*
• Minimal area by using a single comparator. • Single offset cancellation for 3-bit.	• Dummy reversal technique reduces the switching effect.

Overall Architecture

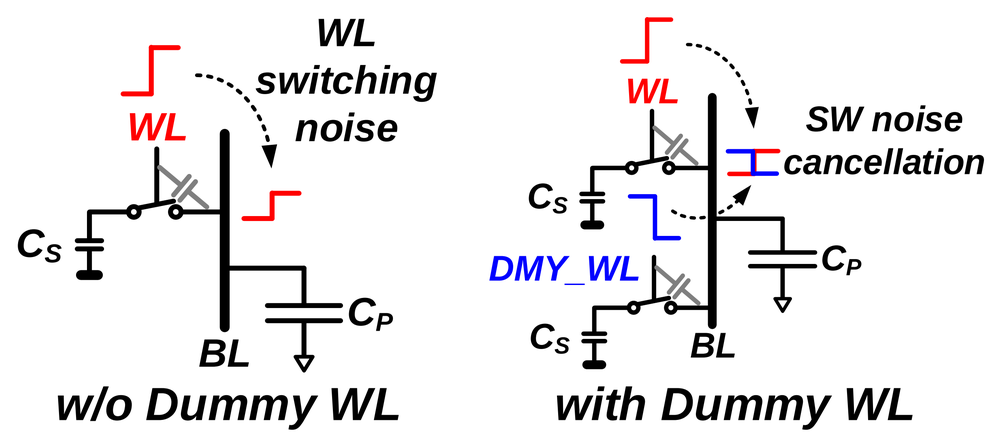
3-bit SAR-Based Offset-Canceled Sense Amplifier

- SAR operation needs only a single comparator, which reduces the overall area for SA.
- Single offset cancellation(OC) for 3-bit decision.



Dummy Reversal Technique

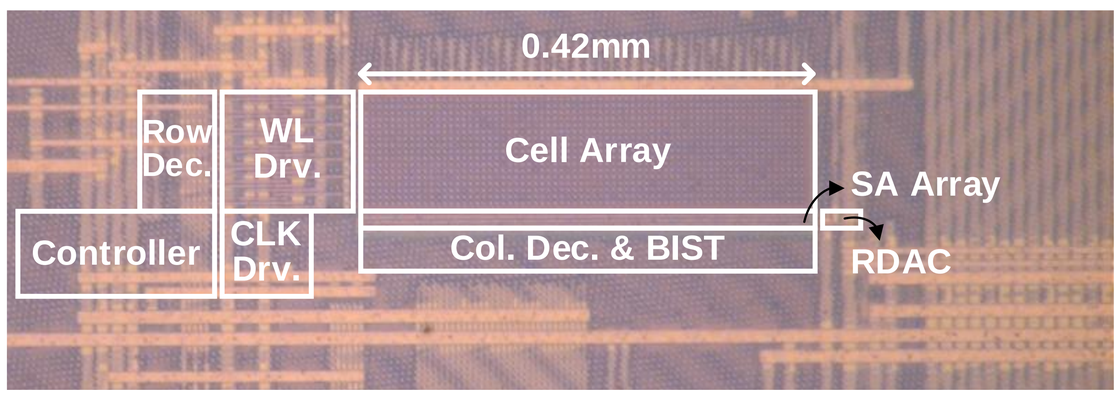
- SA requires single ended operation, which is vulnerable to switching noise.
- Dummy reversal technique reduces the effect of switching noise.



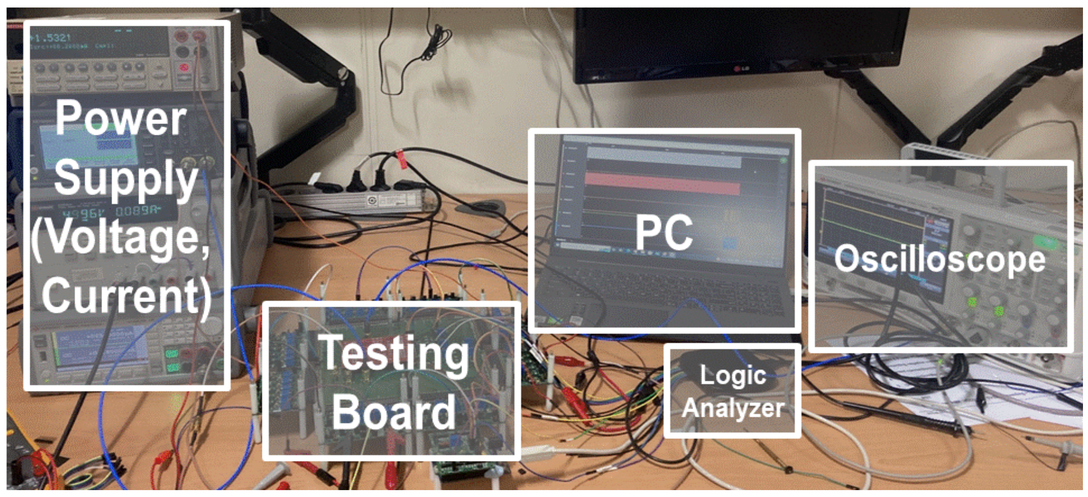
Chip Photo and Simulation/Chip Results

Implemented with TSMC 65nm Technology(HM-2402)

- Cell array(8k) with 64 SAs

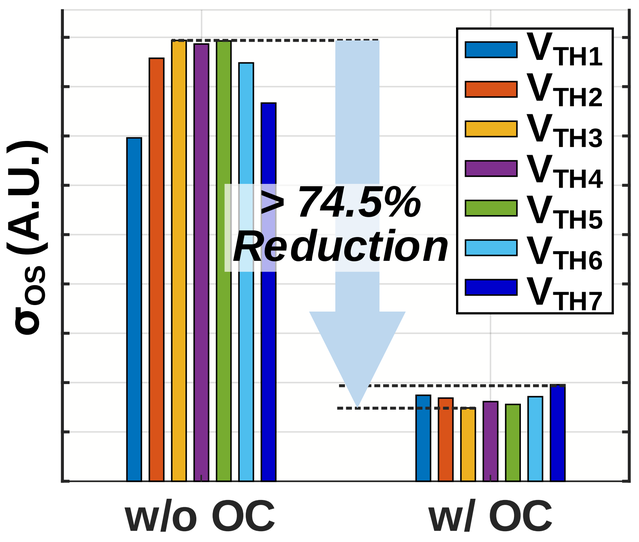


Chip Photo



Measurement Set-up

Measurement Results of SA Offset & Performance Summary



Performance Summary

Process	65nm CMOS
V_{DD}(V)	1
Op. freq. (MHz)	400
Number of bits	3
C_{BL}/C_{CELL}	26.5fF/4.4fF
Power per bit (uW)	3.52

Future Plan

- Improvement of power efficiency for DAC and REF_L

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

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