IDEC Chip Design Contest

Fully-integrated 4-to-1 DC-DC Converter Through Electro-magnetic Coupling

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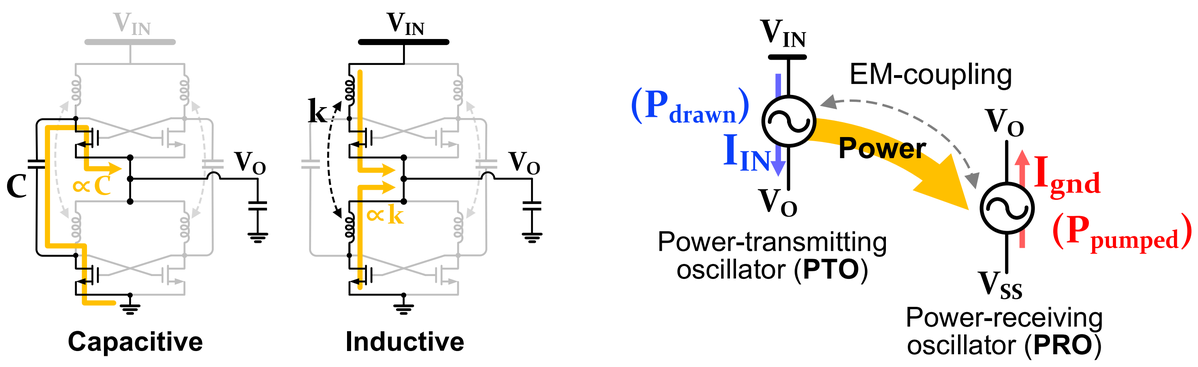
Introduction

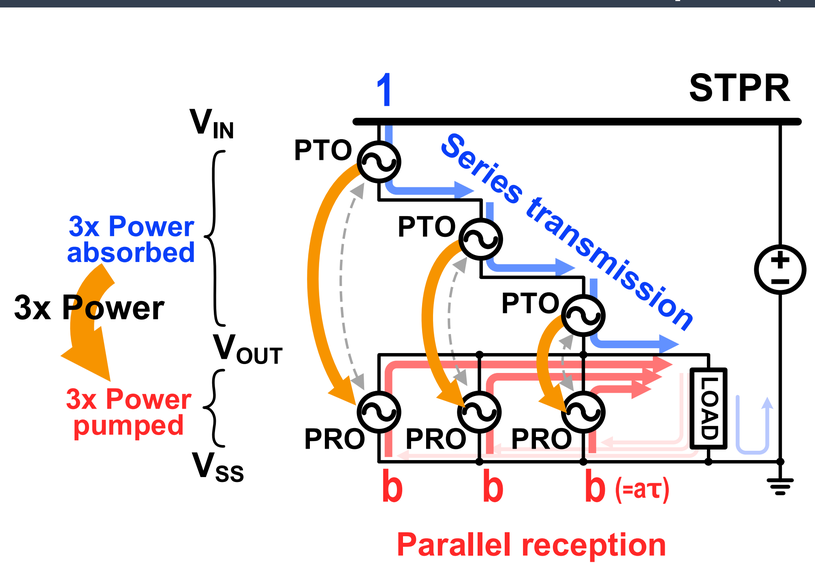
Power management ICs require high conversion ratios to step down voltages from sources such as batteries or USB ports. However, this often results in degraded performance due to increased transfer steps or complex switching. Recent works have addressed these challenges with different trade-offs. A 3:1 resonant switched-capacitor converter [4] achieved 78.3% efficiency but exhibited low power density (16 mW/mm²) due to a f_{sw} of 30MHz. An EMLC-based converter [5] achieved a high power density but was limited to 2:1 conversion and showed only 60.4% efficiency at peak P_{OUT}. To overcome these shortcomings, we propose a series-transmission and parallel-reception (STPR) EMLC architecture with a tuned flying capacitor to suppress charge sharing. Implemented in 28 nm CMOS, the prototype achieves 74.5% efficiency at 0.26 W/mm² and 0.78 W/mm² peak power density at 67.1% efficiency. It also supports 1:4 and 4:3 conversions, with efficiencies of 74.3% and 90.3%, respectively.

Electro-magnetically Coupled Class-D LC Oscillator (EMLC)

Power tansfer mechanism of EMLC

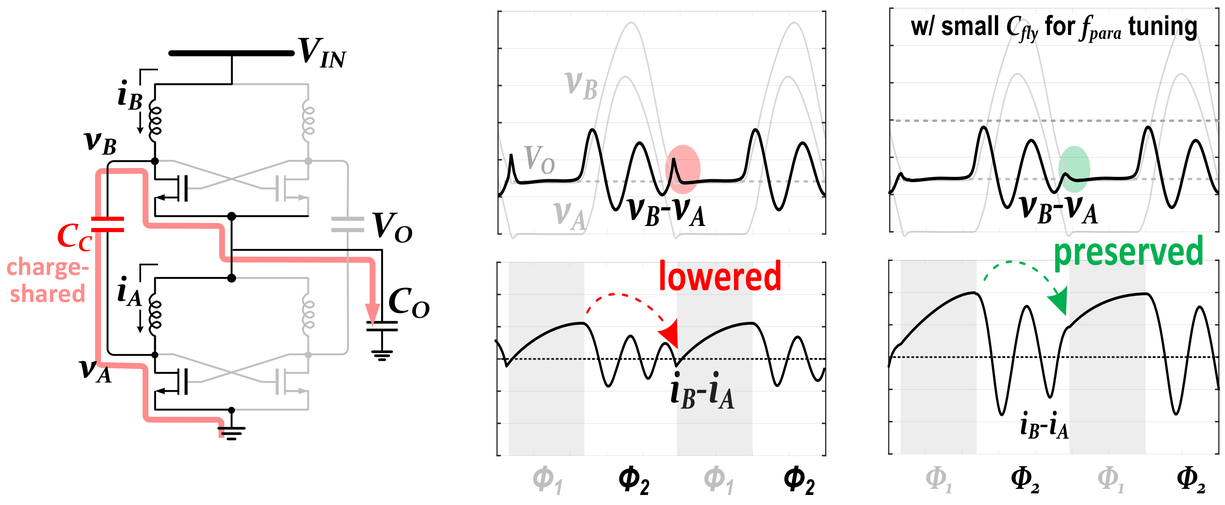


Proposed Series-transmission and Parallel-reception(STPR) EMLC

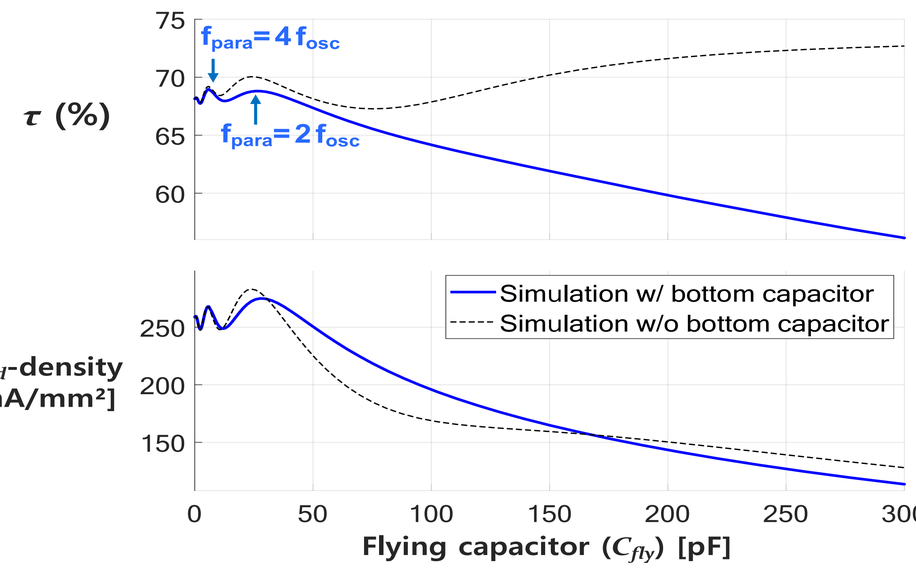


1) PTOs are connected in series, PROs are connected in parallel.
2) High efficiency and power density: Thanks to its single step power transfer, it does not suffer from significant degradation on efficiency and power density as increase the stages.
3) Favorable for high V_{IN}: high input voltage stress is naturally distributed over series-connected PTOs.
4) Scalability: higher conversion ratio can be easily achieved by adding EMLC pairs.

Proposed Series-transmission and Parallel-reception(STPR) EMLC



Chip Photo, Measurement Results



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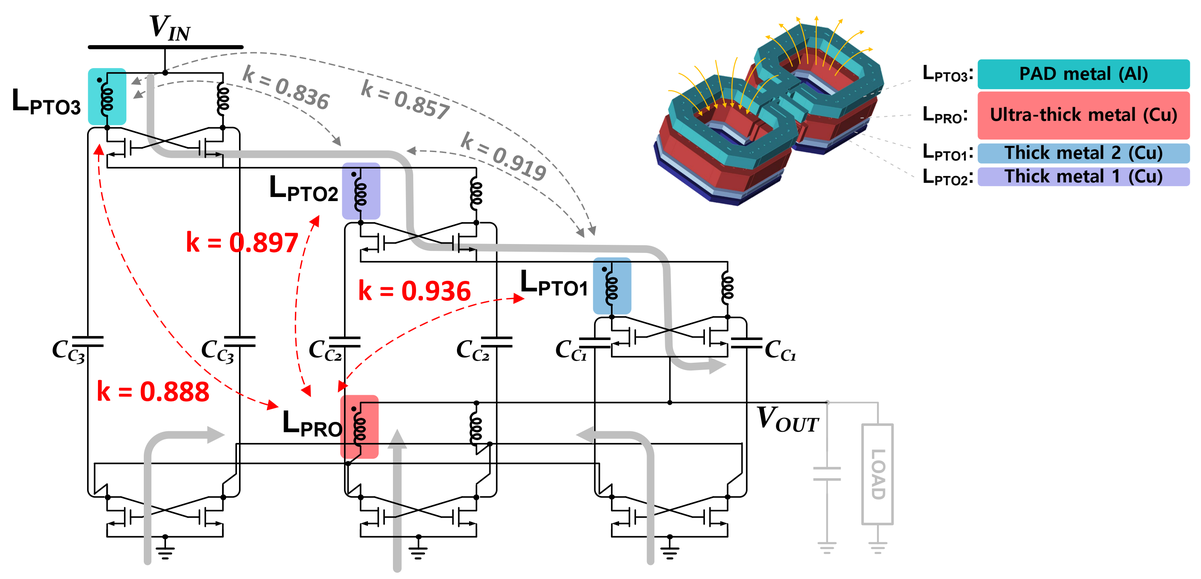
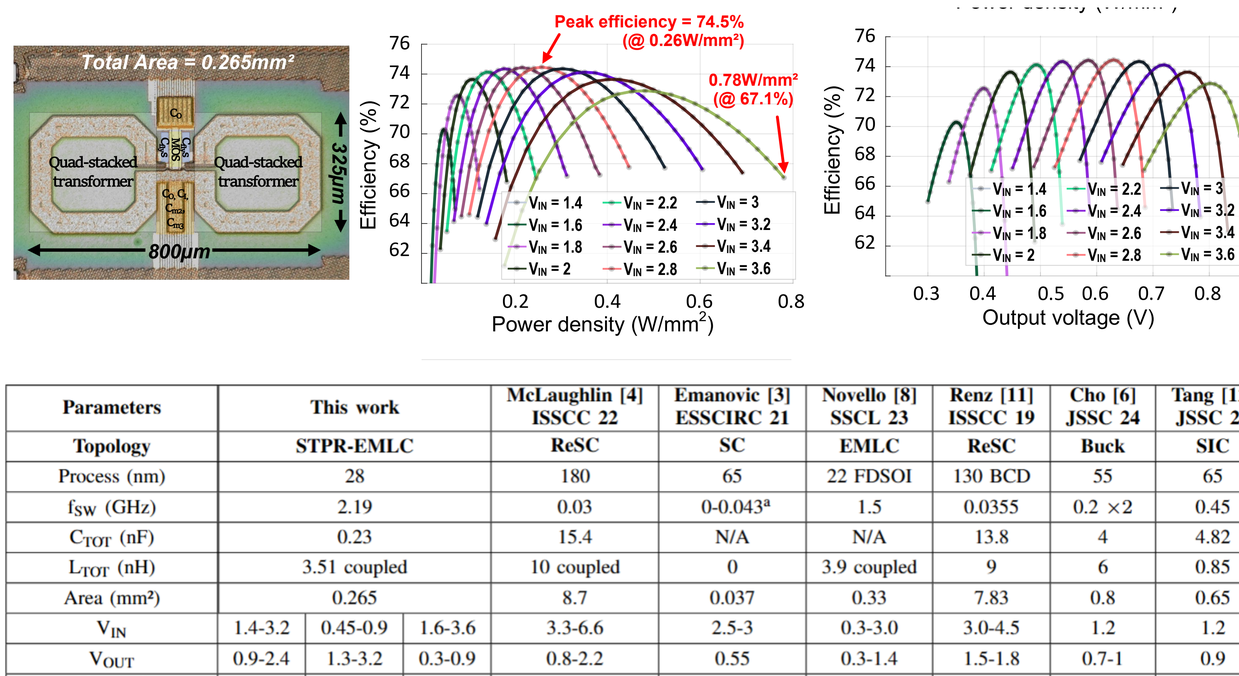


Chip Photo, Measurement Results



Parameters	This work			McLaughlin [4] ISSCC 22	Emanovic [3] ESSCIRC 21	Novello [8] SSCL 23	Renz [11] ISSCC 19	Cho [6] JSSC 24	Tang [12] JSSC 21
Topology	STPR-EMLC			ReSC	SC	EMLC	ReSC	Buck	SIC
Process (nm)	28			180	65	22 FDSOI	130 BCD	55	65
f_{SW} (GHz)	2.19			0.03	0-0.043[a]	1.5	0.0355	0.2 ×2	0.45
C_{TOT} (nF)	0.23			15.4	N/A	N/A	13.8	4	4.82
L_{TOT} (nH)	3.51 coupled			10 coupled	0	3.9 coupled	9	6	0.85
Area (mm²)	0.265			8.7	0.037	0.33	7.83	0.8	0.65
V_{IN}	1.4-3.2	0.45-0.9	1.6-3.6	3.3-6.6	2.5-3	0.3-3.0	3.0-4.5	1.2	1.2
V_{OUT}	0.9-2.4	1.3-3.2	0.3-0.9	0.8-2.2	0.55	0.3-1.4	1.5-1.8	0.7-1	0.9
Nominal Conversion Ratio	**4:3**	**1:4**	**4:1**	**3:1**	**4:1**	2:1	2:1	4:3	4:3
@ Peak Efficiency	**90.3%**	**74.3%**	**74.5%**	**78.3%**	**62%**	**77%**	**85%**	**79.1%**	**78%**
P_{den}(W/mm²)	**0.75**	**0.26**	**0.26**	**0.016**	**0.0026**	**1.5**	**0.033**	**0.90**	**0.55**
EEF [b]	21.5%	-	69.8%	62.1%	66%	40.1%	45.7%	5.2%	3.9%
@ Peak P_{den}(W/mm²)	**3.27**	**0.68**	**0.78**	**0.077**	**0.0026**	**4.1**	**0.033**	**0.9**	**0.73**
Efficiency	**83.3%**	**67.1%**	**67.1%**	**61%**	**62%**	**60.4%**	**85%**	**75.2%**[a]	**74.6%**
EEF [b]	23.5%	-	71.7%	65.7%	66%	-	45.7%	2.7%	-0.5%

[a] Extracted data from the plot. [b] EEF = $(1-\eta_{LDO}/\eta_{conv}) \times 100$ (%).

Acknowledgement and Reference

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[1] N. Tang et al., "Fully Integrated Buck Converter with 78% Efficiency at 365mW Output Power Enabled by Switched-Inductor Capacitor Topology and Inductor Current Reduction Technique," ISSCC 2019:152-153.

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[3] P. Renz et al., "A Fully Integrated 85%-Peak-Efficiency Hybrid Multi Ratio Resonant DC-DC Converter with 3.0-to-4.5V Input and 500μA-to-120mA Load Range," ISSCC 2019:156-157.

[4] P.H. McLaughlin et al., "A Monolithic 3:1 Resonant Dickson Converter with Variable Regulation and Magnetic-Based Zero-Current Detection and Autotuning," ISSCC, pp. 304-306, Feb. 2022

[5] A. Novello, "A 4.1W/mm2 Peak Power Density and 77% Peak Efficiency Fully Integrated DC-DC Converter based on Electromagnetically Coupled Class-D LC Oscillators and a Resonant LC Flying Impedance in 22nm FDSOI CMOS," VLSI Technology and Circuits 2023:1-2.

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