



# Ka-Band Two-Way Power-Combining Power Amplifier using Merged Inter-stage Transformers

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## Introduction

- Ka-band has recently attracted significant attention due to its potential for
- Simulation results 25-20-✓ Gain (dB) : 21.8–24.3 15-S-parameter (dB) ✓ P<sub>SAT</sub> (dBm) : 21.5–21.8 10-✓ OP1dB (dBm) : 19.6–20.1 ✓ Peak-PAE (%): 34.0–37.7 -10 -15-S22 S21 -20 -25 25 20 35 30 40 Freq. (GHz) 22.0 -42 Gain 21.8 -40 **%** 30<sup>-</sup> AE (%) AE PSAT (dBm) 25 21.6 20 Š eak-P 21.4 (a) 15-(b) 10-Gain -34 <sup>**D**</sup> 21.2 21.0*+* 26 32 12 14 16 18 20 22 10 32 28 29 27 30 31 Output power (dBm) Frea. (GHz) Fig. 4, Simulation results

**Simulation Results** 



high-capacity wireless communication and radar applications.

- For such applications, high-output-power power amplifiers (PAs) are essential to ensure sufficient transmission range and signal integrity.
- This work demonstrates a two-way power combining technique using merged inter-stage transformers to enhance output power.

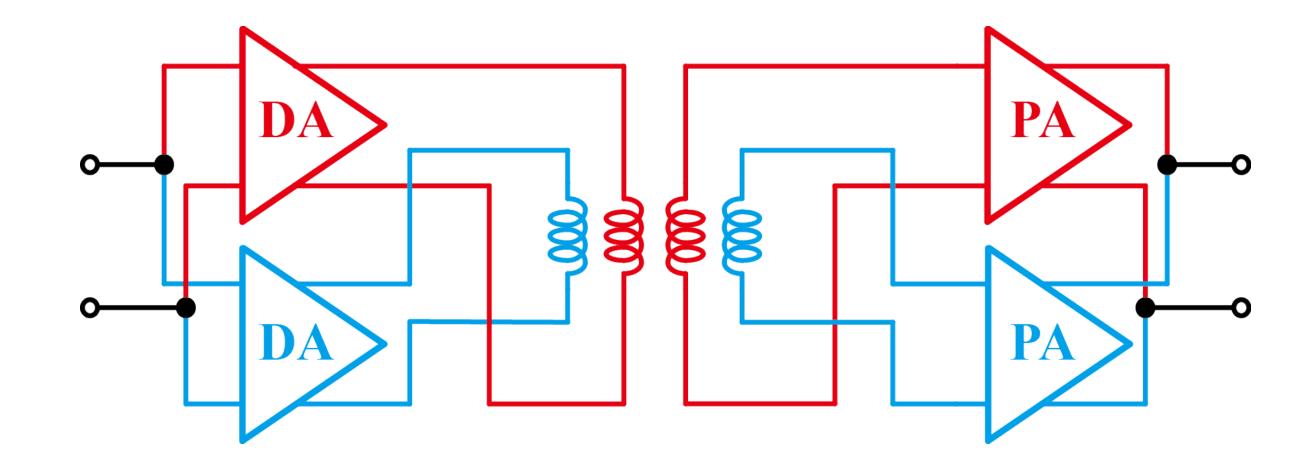
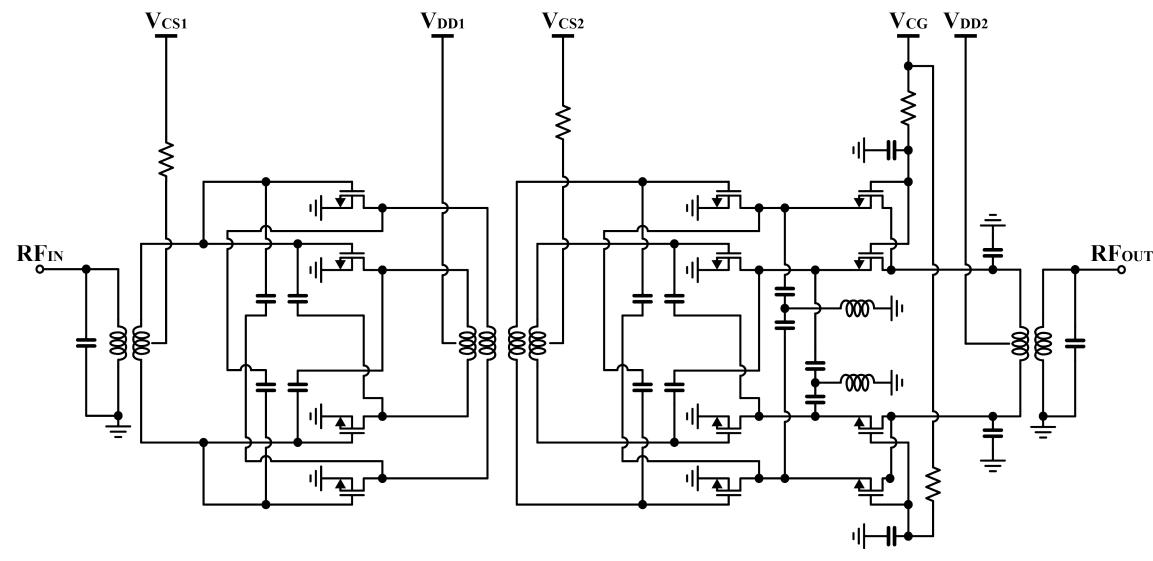


Fig. 1, Block diagram of two-way power combining using a merged inter-stage transformers

## **Circuit Design**

Conclusion

- Frequency : 27–31 GHz
- Topology : 2-stage Diff.-to-Diff.
- Applied Technique :
  - Merged inter-stage transformers were used to achieve high output power while enabling compact two-way power combining.
  - ✓ A cascode structure was employed in the power stage to achieve both high gain and high output power.
  - ✓ Neutralization capacitors were applied to both the driver and power stages to enhance gain and ensure stability.



Ref.	This work (Sim.)	[1]	[2]	[3]
Tech.	28nm	65nm	28nm	65nm
Architecture	2-way	2-way	1–way	1–way
Freq. (GHz)	27–31	12.3–15.6	28	28
Gain (dB)	21.8–24.3	26–27.3	20.5	18
P <sub>SAT</sub> (dBm)	21.5–21.8	23–23.4	18.1	18.5
OP1dB (dBm)	19.6–20.1	22.7–22.9	16.8	N/A
Peak-PAE (%)	34.0–37.7	22.7–22.9	41.5	27.3
Core Area (mm <sup>2</sup> )	0.195	0.23	0.28	0.14

- The two-way power combining power amplifier with high output was designed using power merged inter-stage transformers, achieving a compact chip size.
- The fabricated chip has been

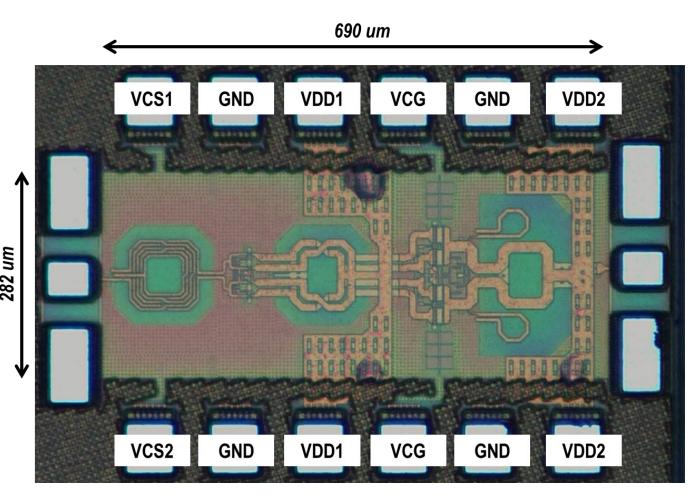


Fig. 5, Microphotograph of the two-way PA

#### Fig. 2, Full schematic of the two-way PA using merged inter-stage transformers

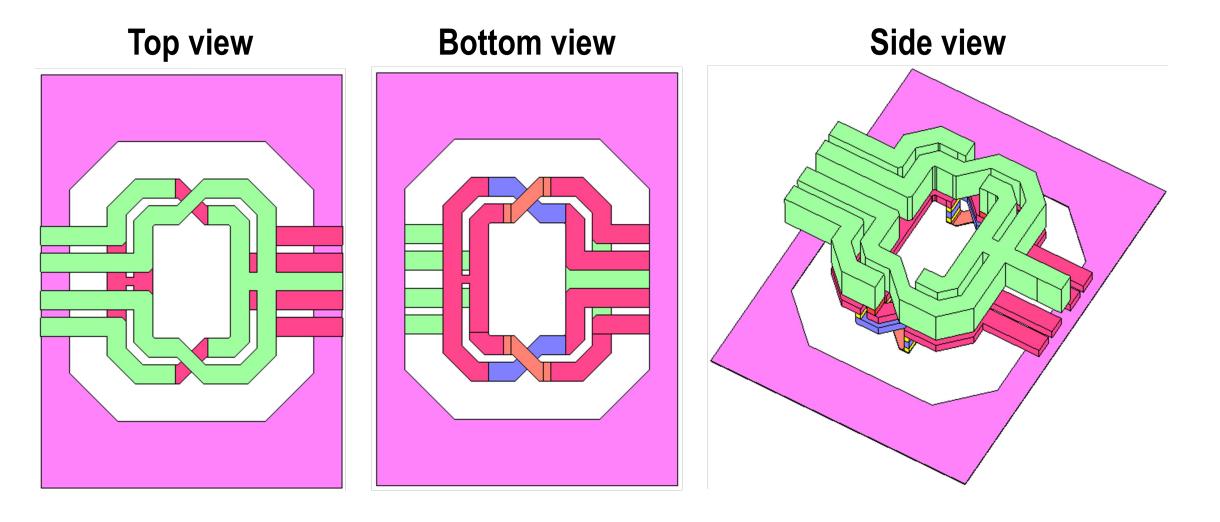
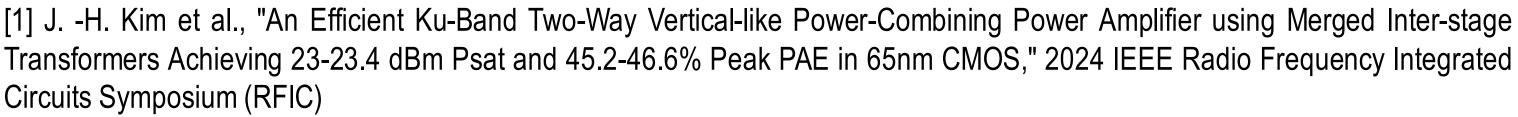


Fig. 3, Layout of the merged inter-stage transformers

received and is currently being prepared for on-chip probing measurements.

### Reference



[2] B. Park et al., "Highly Linear mm-Wave CMOS Power Amplifier," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 12, pp. 4535-4544, Dec. 2016, doi: 10.1109/TMTT.2016.2623706.

[3] S. Lee, S. Kang and S. Hong, "A 28-GHz CMOS Linear Power Amplifier With Low Output Phase Variation Over Dual Power Modes," in IEEE Microwave and Wireless Components Letters, vol. 29, no. 8, pp. 551-553, Aug. 2019, doi: 10.1109/LMWC.2019.2922507.

### Acknowledgement

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