IDEC Chip Design Contest

A Power-efficient Incremental Delta-Sigma Analog-to-Digital Converter with CT Input Stage for Sensor Applications

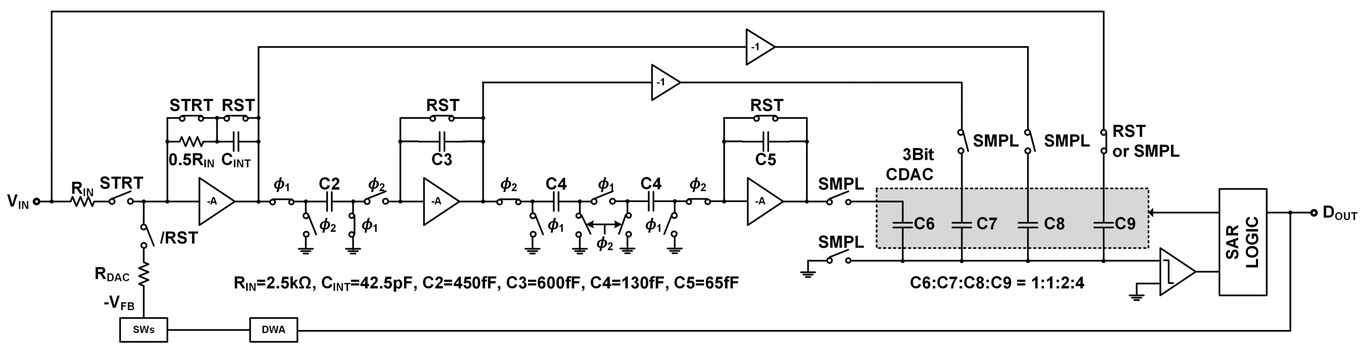
Kwan-Hoon Song and Seung-Tak Ryu
Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea
Mixed-Signal Integrated Circuits Laboratory (MSICL), khsong@kaist.ac.kr

Abstract

This work presents a high-resolution incremental delta-sigma ADC (hybrid CT-DT I-DS ADC) with CT input stage for sensor readout and measurement instruments. As an incremental ADC with the architecture utilizing CT input stage, it achieves 16-bit resolution and supports input multiplexing via reset operation while providing easier input drivability. The loop filter (LF) adopts a third-order structure with the first integrator in CT and the second and third in DT, preserving the anti-aliasing and resistive input benefits of the CT stage while minimizing overall power consumption. A Class-AB amplifier is used in the first integrator, and cascaded floating inverter amplifiers (FIAs) are used in the second and third stages to improve power efficiency. To reducing the first-sample error and allowing the fast LF settling, precise timing of input pre-conversion is utilized. The I-DS ADC achieves a Schreier FoM of 170 dB, with an SNDR of 97.1 dB in a 10 kHz bandwidth, consuming 515 μW from a 1 V supply.

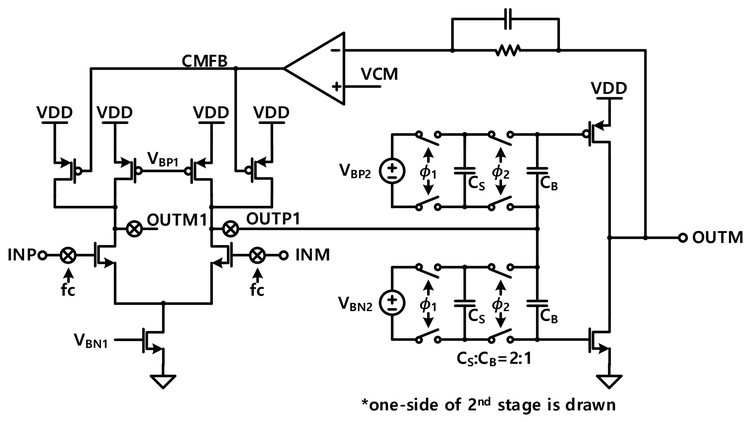
Proposed Architecture & Measurement Results

■ Overall Architecture



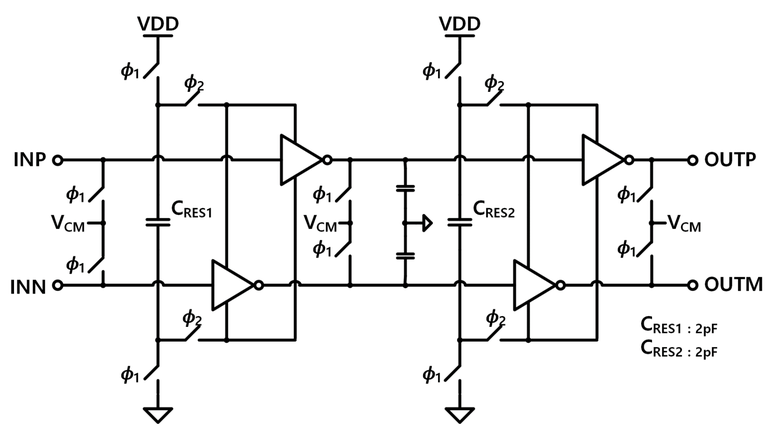
- **First CT Integrator**
  - Resistive input impedance → Reducing drivability burden of AFE ☺
  - Anti-aliasing → Reducing the noise folding resulted from sampling ☺
  - Passive-ELD compensation → Simplified layout and better matching ☺
- **Fully Dynamic DT integrators**
  - Two-stage FIA (floating inverter amplifier) → High power efficiency ☺
  - Charge sharing of feedforward signals → Output swing requirement↓ ☺

■ Amplifier Design



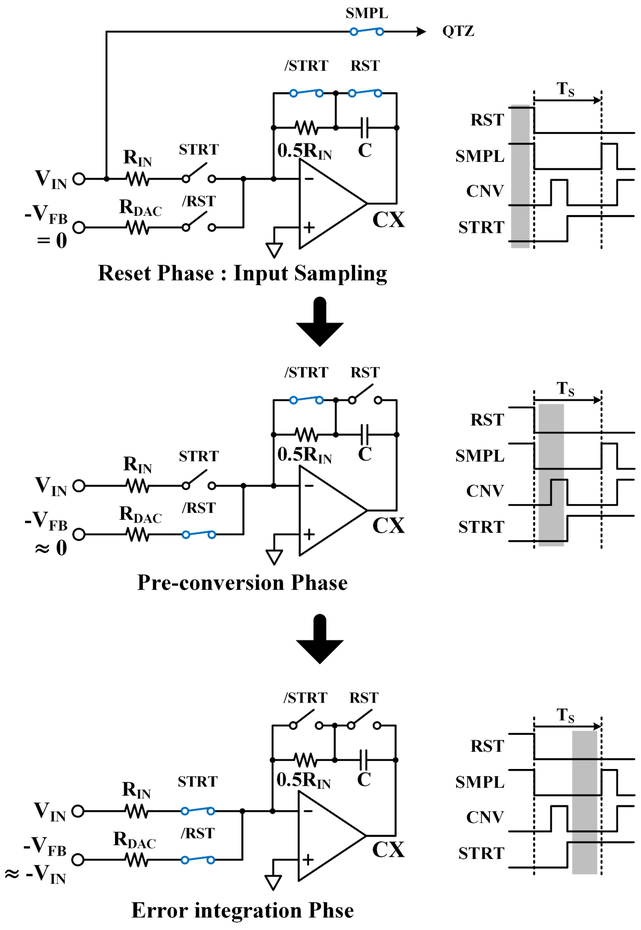
*one-side of 2nd stage is drawn

- **Amplifier for First Integrator**
  - Class-AB output stage → Linearity, high gain ☺
  - Dynamic Bias for 2nd stage → Low V_{OP} ☺
  - Chopping → flicker noise ↓ ☺



- **Amplifier for Second and Third Integrators**
  - Two-stage FIA → output signal swing range ↑ ☺
  - Local CMFB → constant output CM w/o large C_M ☺
  - w/o large C_M → stability ↑ ☺

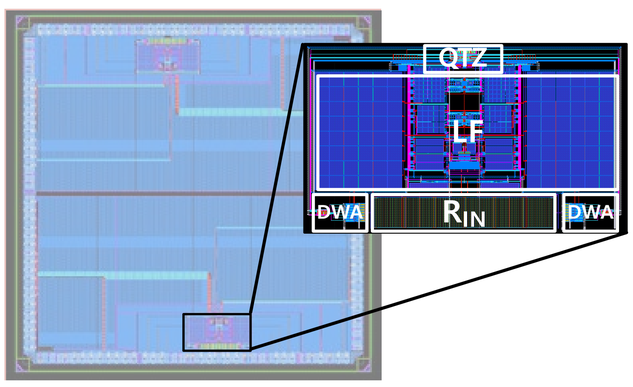
■ Input Pre-conversion



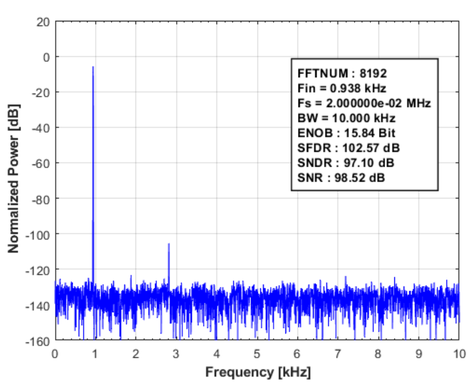
- **Input pre-conversion**
  - Accurate incremental operation ☺
  - Fast settling of loop filter ☺
  - No waste of conversion results ☺

■ Chip Layout & Measurement Results

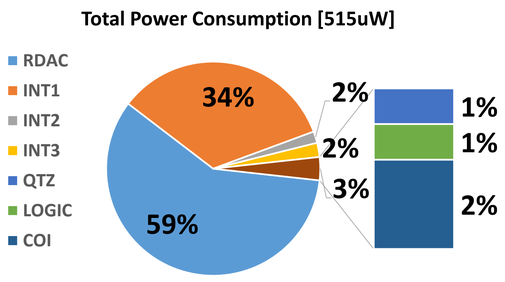
■ Layout



■ FFT Plot



■ Power Breakdown



Conclusion

This work presents an incremental ΔΣ ADC architecture with a continuous-time (CT) input stage to leverage its resistive input impedance and reduce the design requirement of analog front-end. Discrete-time (DT) stages are used to enhance power efficiency. A floating inverter amplifier (FIA) in the DT stages and a low-voltage Class-AB amplifier in the CT stage provide high linearity while reducing power. An input pre-conversion sequence enables fast loop filter settling. The ADC achieves a peak SNDR of 97.1 dB over a 10 kHz bandwidth with 515 μW power consumption, resulting in a Schreier FoM of 170 dB.