

Comparison of RF characteristics of transistors using CMOS 28 nm process

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Introduction

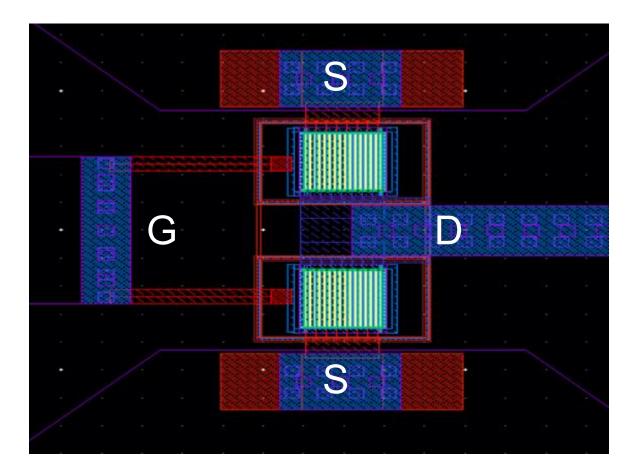
Millimeter-wave circuits require special design considerations due to significant parasitic effects at high frequencies. These parasitics depend on transistor size and layout, impacting RF performance. This study evaluates various 28 nm CMOS transistors using S-parameter measurements to identify optimal structures for 5G millimeter-wave applications.

Results

m3	m4
freq=40.00GHz	freq=40.00GHz
max_1=9.792	de_embed_extraction_s28n_comp1max_1=10.132
m1	m2
freq=28.00GHz	freg=28.00GHz

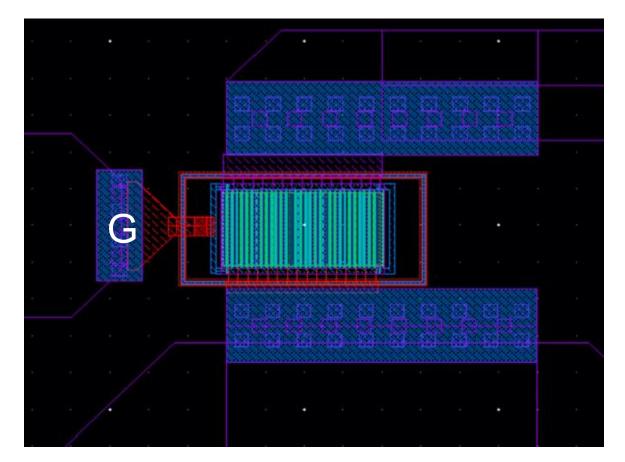
m3	m4
freq=40.00GHz	freq=40.00GHz
max_1=5.979	de_embed_extraction_s28n_comp1max_1=8.977
m1	m2
freq=28.00GHz	freq=28.00GHz

Design

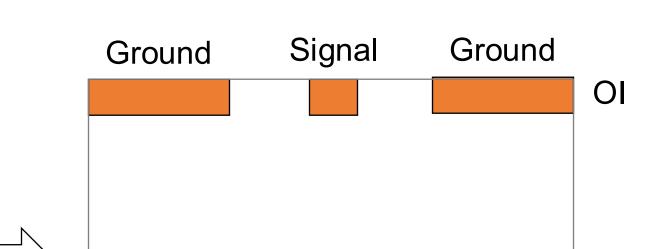


< Symmetry type >
Symmetry type & Ring type Layout

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< Ring type >



OI

M2

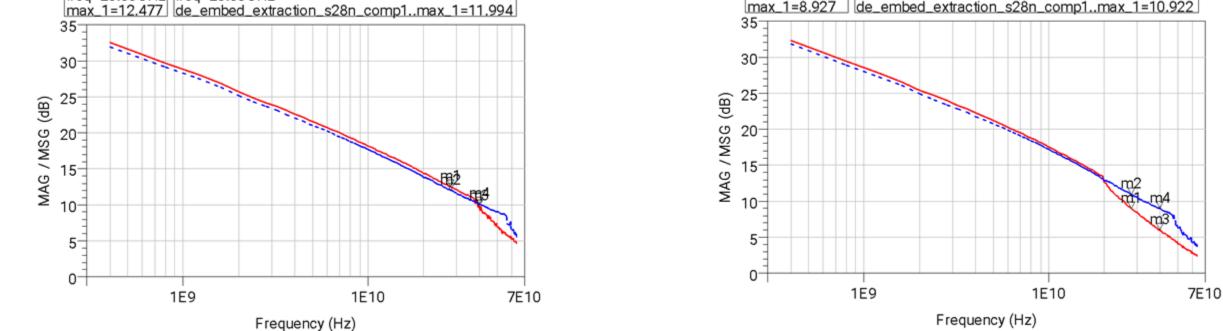
M1

OI

IB

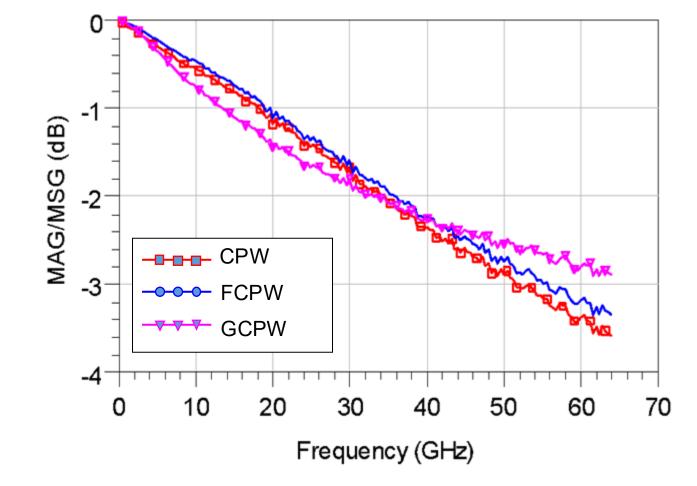
M2

M1



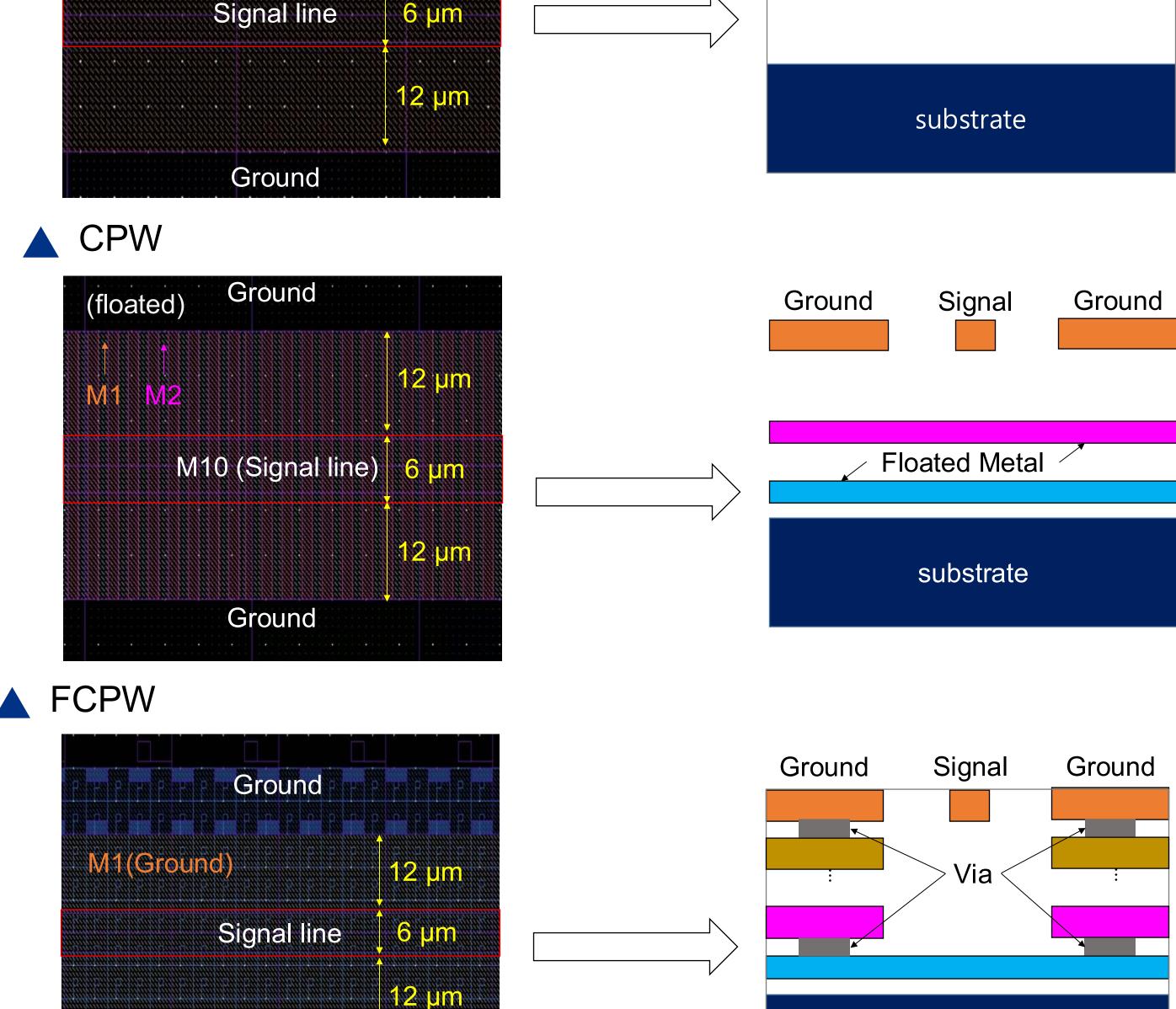
left - 2×32 µm, right - 2×64 µm, solid line: lvt nfet_rf, dotted line: nfet_rf, all ring-shaped structures

Comparison of MAG/MSG characteristics according to threshold voltage

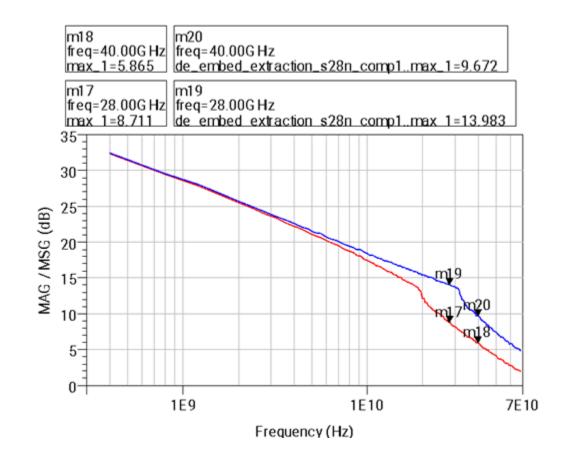


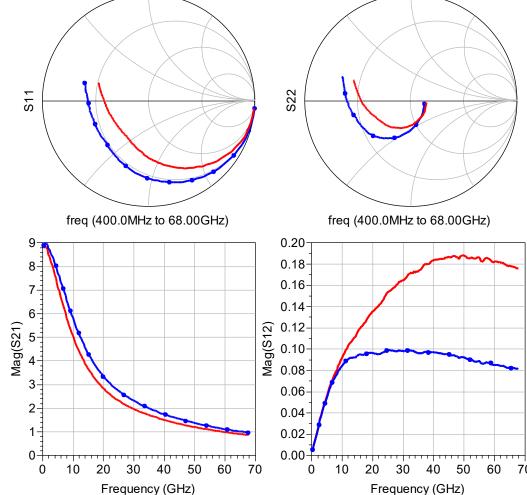
This graph compares the MAG/MSG characteristics of different CPW types. Both CPW and GCPW show better performance than FCPW up to 40 GHz, but FCPW outperforms them beyond 40 GHz. Based on these results, CPW or FCPW is

Comparison of MAG/MSG characteristics according to CPW Type



preferable for low-frequency applications, while GCPW is more suitable at higher frequencies.





left: MAG/MSG, right: S-parameters

Measurement results of ring type (solid) and symmetry type (circle) - $2 \times 64 \mu m$ Devices with the same size ($2 \times 64 \mu m$) were compared under identical bias for optimal RF performance. The symmetry type showed ~4 dB higher MAG/MSG due to lower gate/drain resistance (S11) and smaller S12, confirming its superior RF characteristics.

Conclusions

This study evaluates 28 nm CMOS transistors for 5G mmWave circuits. S-parameter measurements up to 67 GHz show that symmetric layout provide the best MAG/MSG. Despite application-dependent parasitics and power, high-frequency gain is critical for optimal transistor selection. The CPW layout also affects performance, with different structures favored at different frequencies.



substrate

GCPW

GCPW

Uses M1 as ground, with VIAs connecting from M1 to the top layer (OI)

the substrate is not used as ground.

FCPW

Floating CPW formed between M1 and M2, with no ground connection. **CPW**

Standard CPW using the substrate as ground.

Acknowledgment

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References

Kim, Jihoon, and Youngje Sung. "Triple-Stacked FET Distributed Power Amplifier Using 28 nm CMOS Process." *Electronics* 13.22 (2024): 4433.



