Chip Design Contest

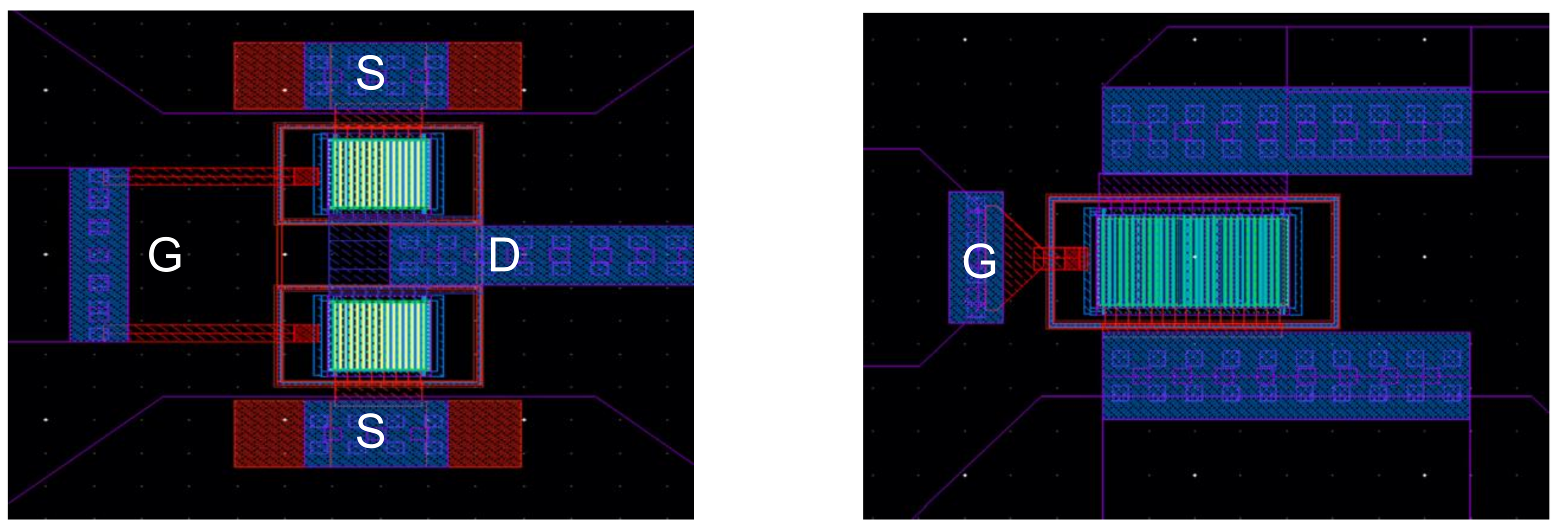
Comparison of RF characteristics of transistors using CMOS 28 nm process

Hosung Kang, Seungyoon Han and Jihoon Kim
School of Electronic Engineering, Kyonggi University, Korea

Introduction

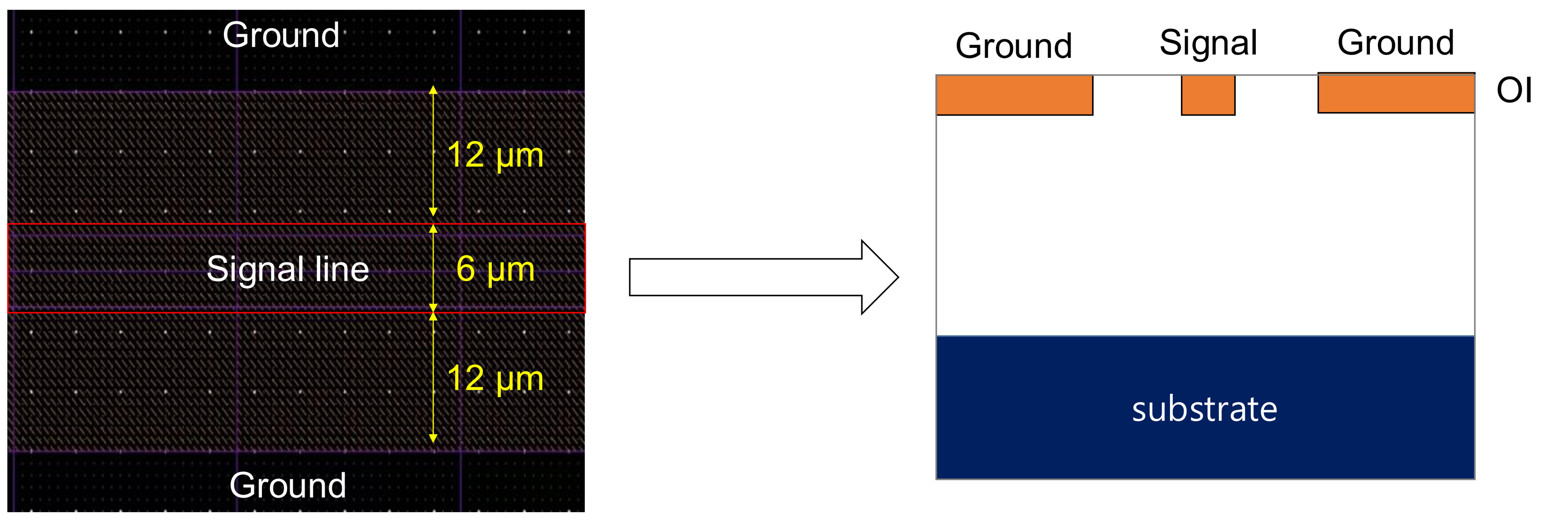
Millimeter-wave circuits require special design considerations due to significant parasitic effects at high frequencies. These parasitics depend on transistor size and layout, impacting RF performance. This study evaluates various 28 nm CMOS transistors using S-parameter measurements to identify optimal structures for 5G millimeter-wave applications.

Design

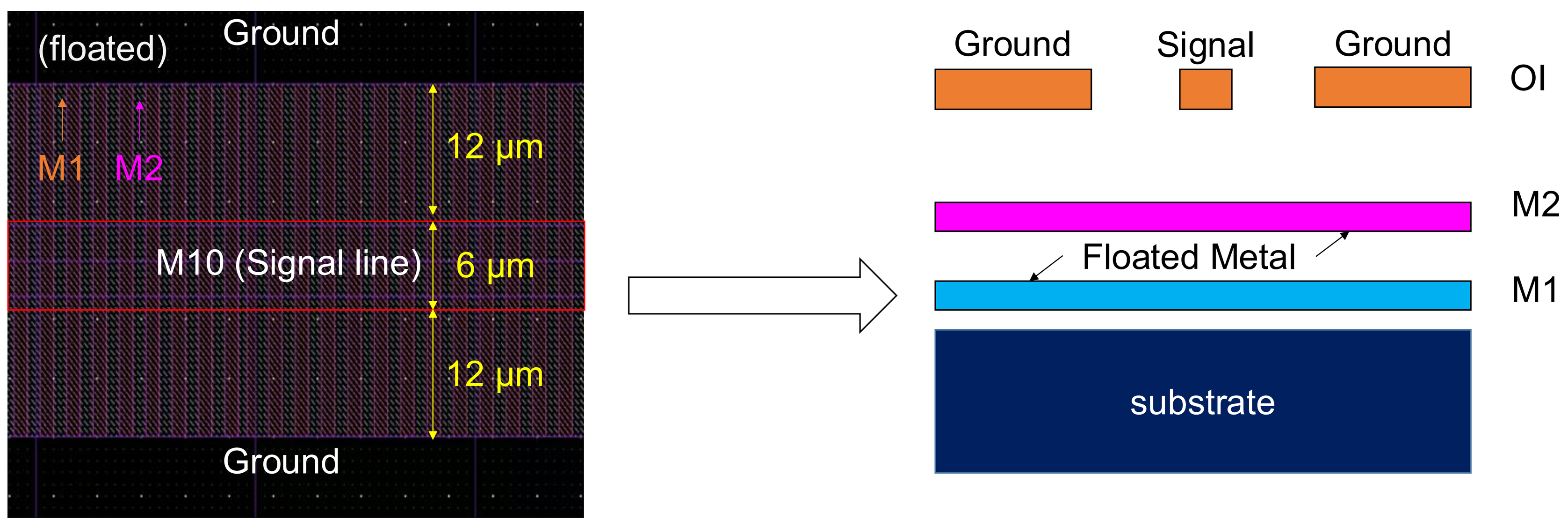


< Symmetry type > < Ring type >

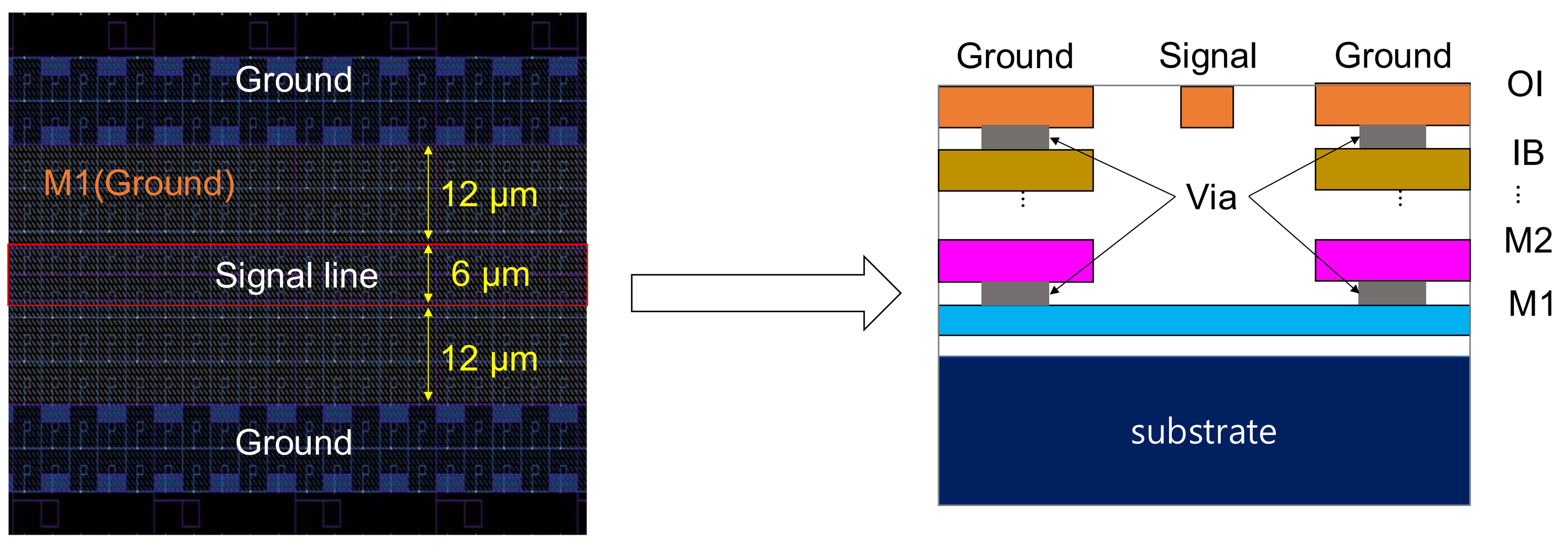
▲ Symmetry type & Ring type Layout



▲ CPW



▲ FCPW



▲ GCPW

GCPW

Uses M1 as ground, with VIAs connecting from M1 to the top layer (OI) the substrate is not used as ground.

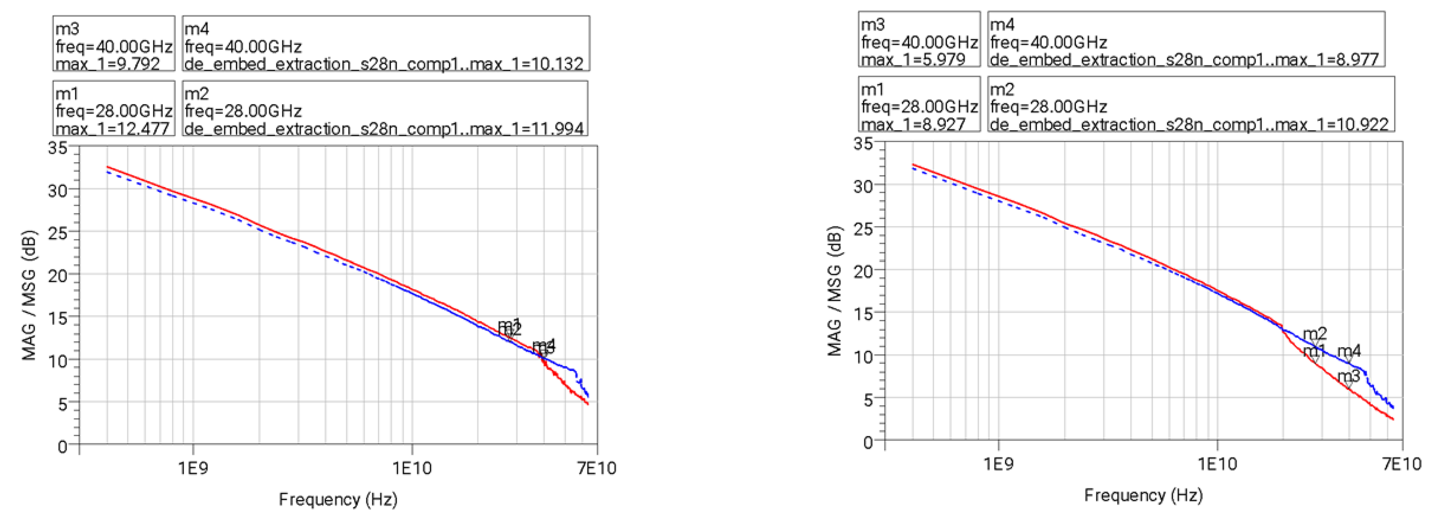
FCPW

Floating CPW formed between M1 and M2, with no ground connection.

CPW

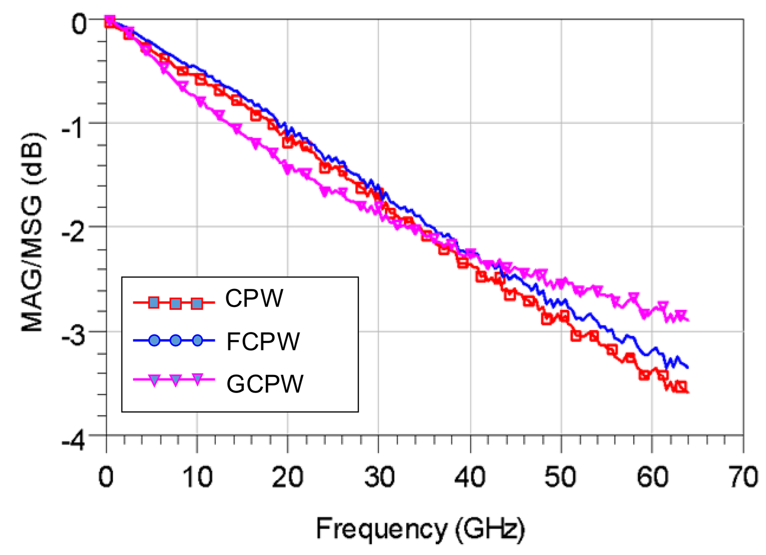
Standard CPW using the substrate as ground.

Results



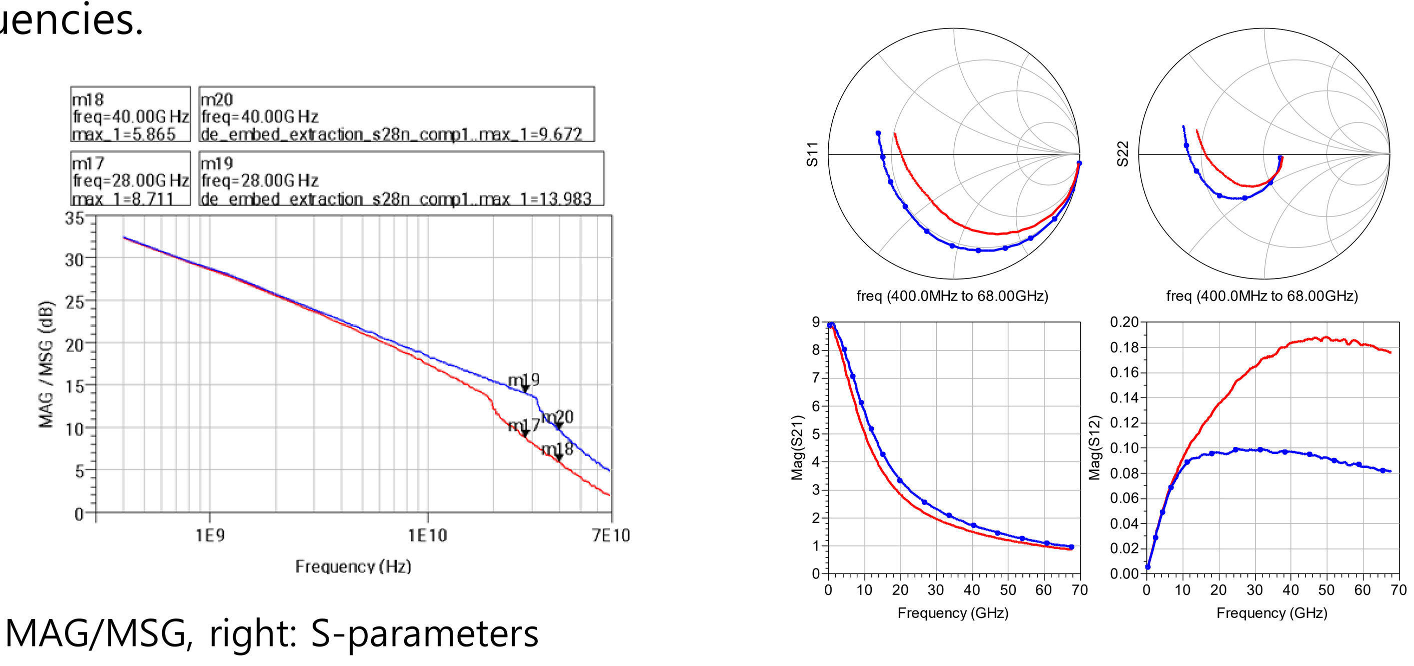
left - 2×32 μm, right - 2×64 μm, solid line: lvt nfet_rf, dotted line: nfet_rf, all ring-shaped structures

▲ Comparison of MAG/MSG characteristics according to threshold voltage



▲ Comparison of MAG/MSG characteristics according to CPW Type

This graph compares the MAG/MSG characteristics of different CPW types. Both CPW and GCPW show better performance than FCPW up to 40 GHz, but FCPW outperforms them beyond 40 GHz. Based on these results, CPW or FCPW is preferable for low-frequency applications, while GCPW is more suitable at higher frequencies.



left: MAG/MSG, right: S-parameters

▲ Measurement results of ring type (solid) and symmetry type (circle) - 2×64 μm

Devices with the same size (2 × 64 μm) were compared under identical bias for optimal RF performance. The symmetry type showed ~4 dB higher MAG/MSG due to lower gate/drain resistance (S11) and smaller S12, confirming its superior RF characteristics.

Conclusions

This study evaluates 28 nm CMOS transistors for 5G mmWave circuits. S-parameter measurements up to 67 GHz show that symmetric layout provide the best MAG/MSG. Despite application-dependent parasitics and power, high-frequency gain is critical for optimal transistor selection. The CPW layout also affects performance, with different structures favored at different frequencies.

Acknowledgment

EDA tool and MPW were supported by the IC Design Education Center (IDEC), Korea

References

Kim, Jihoon, and Youngje Sung. "Triple-Stacked FET Distributed Power Amplifier Using 28 nm CMOS Process." *Electronics* 13.22 (2024): 4433.

KGU

반도체설계교육센터
IC DESIGN EDUCATION CENTER