IDEC Chip Design Contest

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Cryogenic LNA in 28nm CMOS Process for Quantum Computing

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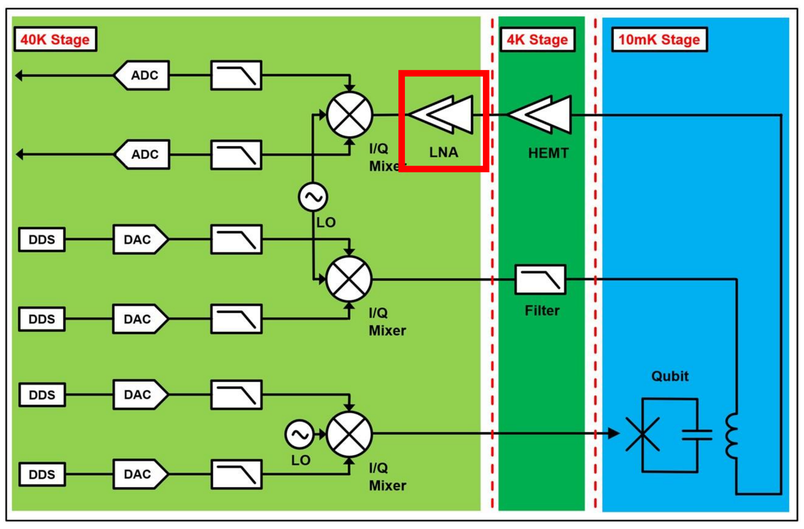
Introduction

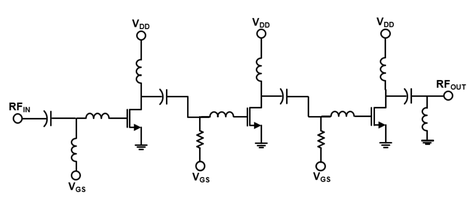
- To maximize scalability, reliability, and computational speed of superconducting quantum computers, we aim to miniaturize current commercially available quantum computing systems, which rely on off-chip measurement instruments, to an on-chip configuration.
- In this research, we developed a Low-noise amplifier (LNA) for the receiver required in a quantum computing system.

Circuit Design

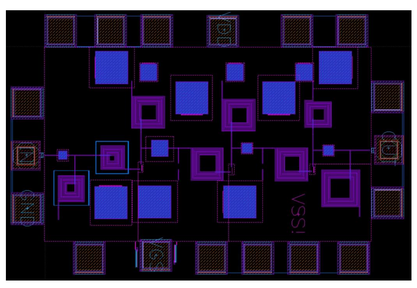


Quantum controller block diagram

- The current implementation of quantum control/readout systems relies on room-temperature measurement instruments such as Keysight, Quantum Machine, Zurich Instruments, leading to issues such as wiring, noise, and cost.
- Integration of circuits for controlling/reading quantum states at ultra-low temperatures requires incorporation into a cryogenic refrigerator.



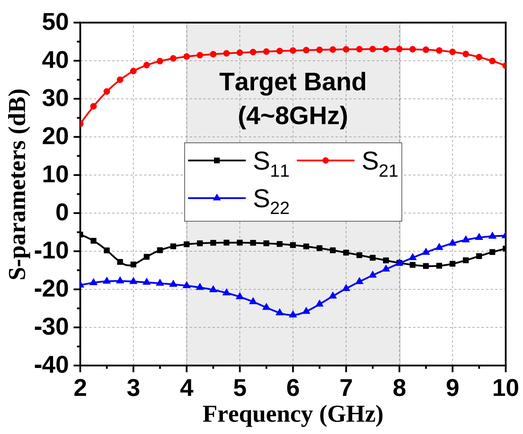
3Stage CS LNA



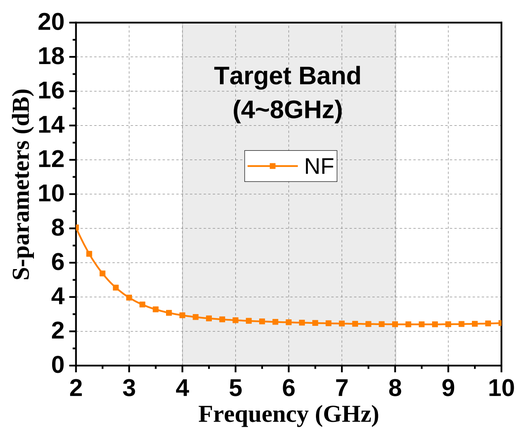
LNA Layout

- Common Source (CS), Common Gate (CG), and Cascode configurations are commonly used in LNA design. In this work, the CS topology was employed to achieve high gain and stability under cryogenic conditions.

Results



S-parameters



Noise Figure

- **This chip is fabricated Samsung 28nm CMOS process.**
- **The 3-dB bandwidth is 6.2 GHz from 3.6 GHz to 9.8 GHz.**
- **Gain is 42 dB and NF is 2.4 dB with 26.65 mW power consumption.**
- **Chip size is 1.8 mm × 1 mm.**

LNA Comparison Table					
Ref.	**Tech.**	**Gain (dB)**	**Bandwidth**	**NF (dB)**	**Power (mW)**
[1]	65nm CMOS	34-38.9	3.9GHz – 5.3GHz	0.147*	23.1
[2]	65nm CMOS	35	3.6GHz – 5.3GHz	0.147*	10.6
[3]	40nm CMOS	58	6GHz – 8GHz	0.59*	66
[4]	40nm CMOS	70	5GHz – 6.5GHz	0.54*	108
[5]	40nm CMOS	42	4.6GHz – 8.2GHz	0.4*	39
This Work	Samsung 28nm CMOS	42	3.6GHz – 9.8GHz	2.4	26.65

* : Noise Figure measured at cryogenic temperatures

[1] S. Das, S. Raman, and J. C. Bardin, “Design and implementation of a 3.9-to-5.3 GHz 65 nm cryo-CMOS LNA with an average noise temperature of 10.2K,” in IEEE MTT-S Int. Microw. Symp. Dig., Jun. 2022, pp. 719–722.

[2] S. Das, S. Raman and J. C. Bardin, "Design and Implementation of a 3.9-to-5.3 GHz 65 nm Cryo-CMOS LNA with an Average Noise Temperature of 10.2K," 2022 IEEE/MTT-S International Microwave Symposium - IMS 2022, Denver, CO, USA, 2022, pp. 719-722, doi: 10.1109/IMS37962.2022.9865392.

[3] B. Prabowo et al., “A 6-to-8 GHz 0.17 mw/Qubit cryo-CMOS receiver for multiple spin qubit readout in 40 nm CMOS technology,” in 2021 IEEE International Solid- State Circuits Conference (ISSCC), vol. 64, 2021, pp. 212–214.

[4] A. Ruffino et al., “A fully-integrated 40-nm 5-6.5 GHz cryo-CMOS system-on-chip with I/Q receiver and frequency synthesizer for scalable multiplexed readout of quantum dots,” in 2021 IEEE International SolidState Circuits Conference (ISSCC), vol. 64, 2021, pp. 210–212.

[5] Y. Peng, A. Ruffino, and E. Charbon, “A cryogenic broadband sub-1-dB NF CMOS low noise amplifier for quantum applications,” IEEE J. Solid-State Circuits, vol. 56, no. 7, pp. 2040–2053, 2021.

The realization of on-chip amplification under cryogenic conditions presented in this work facilitates the development of fully integrated quantum control systems. By eliminating the reliance on bulky room-temperature instrumentation, this approach contributes to the advancement of compact and scalable architectures for quantum computing.