IDEC Chip Design Contest

A 45-fsrms-Jitter D-Band Frequency Synthesizer Using a Subsampling PLL and a Harmonic-Boosting Frequency Multiplier

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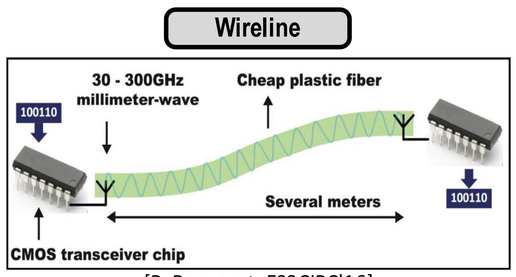
Motivation

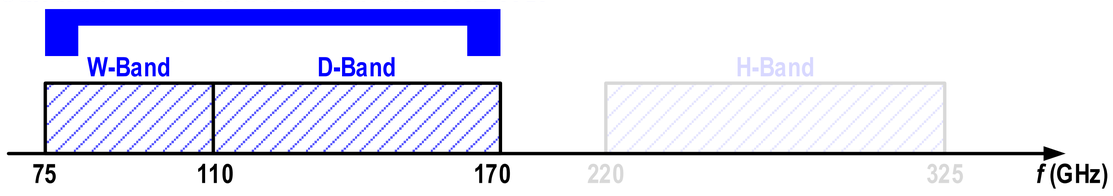
[Smartcitiesworld.net]



[P. Reynaert, ESSCIRC'16]

- Sub-THz bands are gaining attraction for application targeting Tb/s-level data rate either in Wireless or Wireline

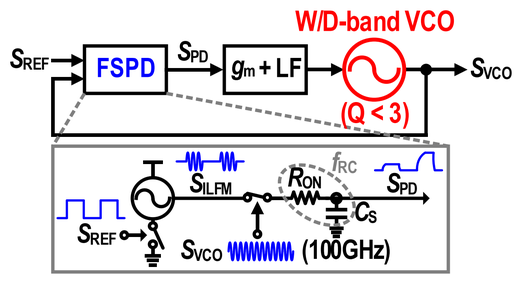
Candidates for CMOS-based Sub-THz TRx



- W/D-bands are the most viable candidates to implement CMOS-based TRx
- Design of a W/D-band freq. synthesizer for LO generation is most critical

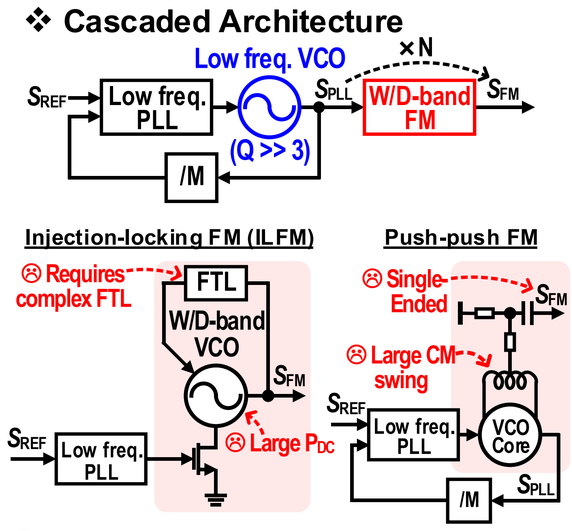
Problems of Prior Architectures

❖ Direct PLL



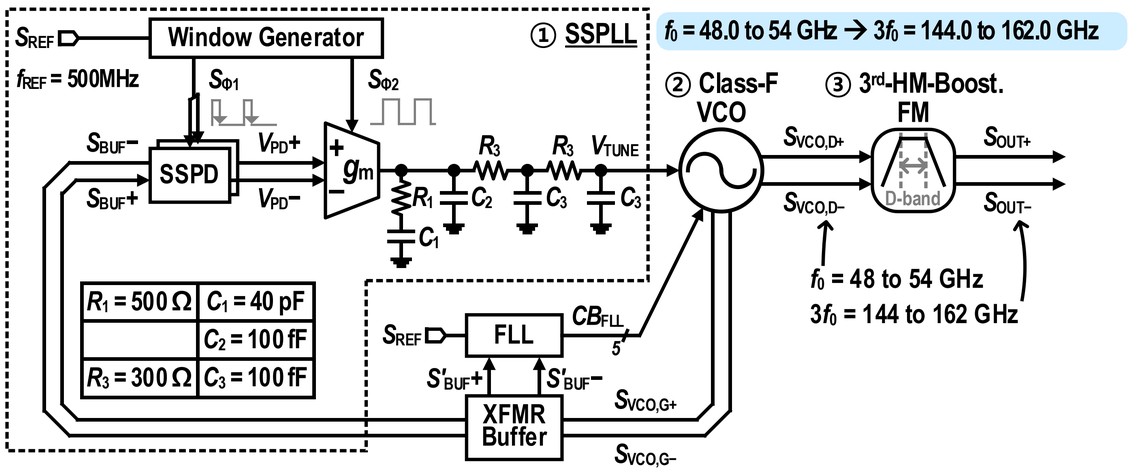
- W/D-bands are the most viable candidates to implement CMOS-based TRx
- Using FSPD, low jitter can be achieved due to high K_{PD} even in W/D-band ☺
- Still very narrow FTR due to large C_{PAR} and low Q of the tank in W/D-band ☹

❖ Cascaded Architecture



- Cascaded architecture can help to achieve both low jitter and wide FTR ☺
- However, there are various disadvantages in conventional W/D-band frequency multipliers ☹

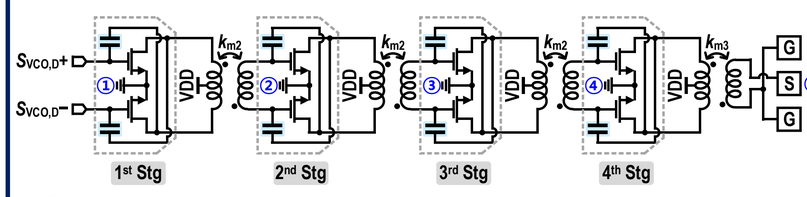
Concept & Overall Architecture

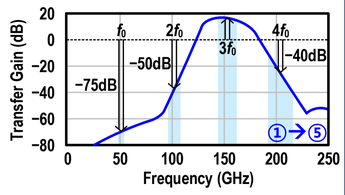


- Cascaded FS: ① SSPLL with ② Class-F VCO and FLL+③ 3rd-HM boost FM
- Low Jitter (< 50fsrms) : ① In-band PN↓ + ② OOB PN↓ + ③ PN Degrad.↓
- Wide FTR (> 10%) : ② FTR & 3rd-HM↑ + ③ P-eff. & BW↑

Key Building Blocks

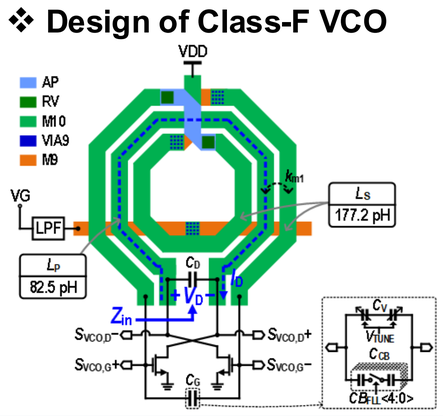
❖ Design of the 3rd-HM Boosting FM

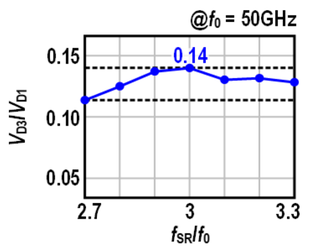


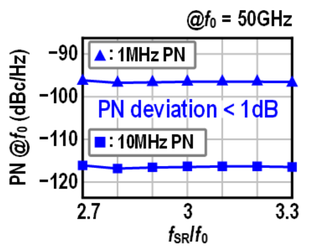


- -75, -50, -40dB suppression at f_0, $2f_0$, and $4f_0$
- Gain higher than 10dB at $3f_0$

❖ Design of Class-F VCO



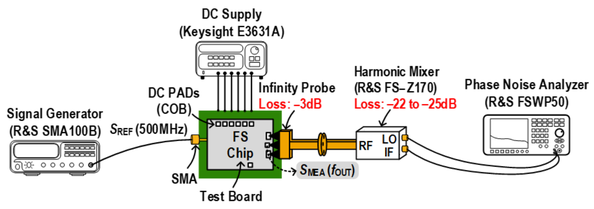




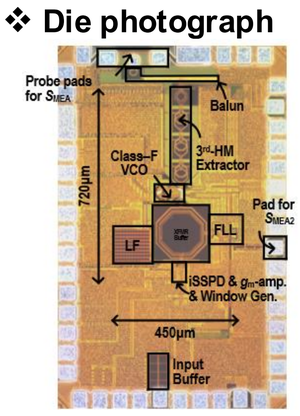
- Sufficiently high $|V_{D3}|/|V_{D1}|$ maintained
- Less than 1dB degradation of PN

Measurement Results

❖ Measurement setting



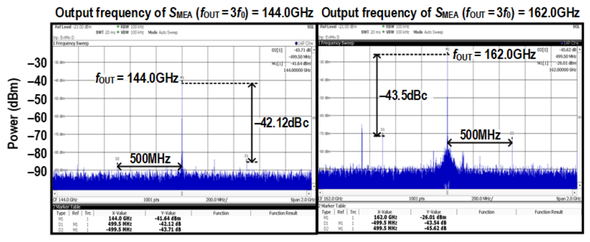
❖ Die photograph



Power Consumption (mW)		
PLL (28.4)	Class-F VCO	13.1
	XFMR Buffer	7.4
	iSSPD & g_m-amplifier	2.2
	Window Generator	1.0
	FLL	4.7
3rd-HM Extractor		37.5
Total		65.9

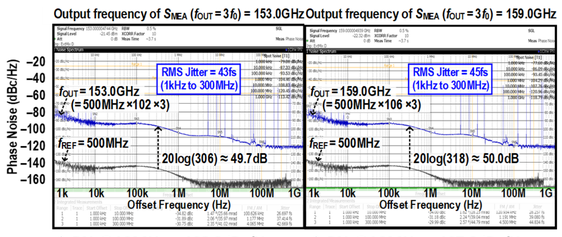
- 40nm CMOS
- Active area: 0.19mm²

❖ Measured spectrum



❖ Reference spur @144.0GHz: −42.1dBc ❖ Reference spur @162.0GHz: −43.5dBc

❖ Measured phase noise



❖ PN @10MHz: −108.8dBc/Hz ❖ PN @10MHz: −107.8dBc/Hz

❖ RMS jitter: 43fs ❖ RMS jitter: 45fs

Performance Comparison

	This Work	JSSC'20 [3] X. Liu	RFIC'14 [4] Y. Chao	TMTT'16 [5] N. Kim	JSSC'19 [9] Z. Huang	ISSCC'21 [1] S. Yoo	ISSCC'23 [2] J. Bang
Process	40 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Architecture	50 GHz SSPLL + 3rd-HM-Boosting FM	23 GHz PLL + ILFM chains	50 GHz PLL + push-push(x2)	61 GHz PLL + push-push(x2)	ADPLL w/ inductively tuned VCO	Direct Fundamental Sampling PLL	Direct Fundamental Sampling PLL
Output freq., f_{OUT} (GHz)	144.0 to 162.0	122.4 to 136.8	96.8 to 108.5	120.4 to 123.8	82.0 to 107.6	99.5 to 102.5	99.5 to 103.5
Tuning Range	**11.8%**	**11.1%**	**11.5%**	**2.78%**	**27.0%**	**2.97%**	**3.94%**
Ref. freq., f_{REF} (MHz)	500	100	195	59.6	125	500	500
100kHz/ 10MHz PN (dBc/Hz) Normalized to 150GHz	−94.4/ −120.7	−83.6/ −94.0	−80.4/ −101.4*	−61.2*/ −100.6	−81.3*/ −101.1*	−93.7/ −97.8	−93.0/ −106.0
$Jitter_{RMS}$, σ_{RMS} (fs) @f_{OUT} (GHz) (Integration range)	**45 @159.0 (1k to 300MHz)**	**159 @132.0 (10k to 10MHz)**	**170* @99.4 (10k to 10MHz)**	**965* @122.0 (10k to 100MHz)**	**276 @107.6 (10k to 10MHz)**	**82 @102.0 (1k to 300MHz)**	**47 @103.5 (1k to 300MHz)**
Reference Spur (dBc)	**−43**	**−33**	**−34***	**−30***	**< −34**	**−42**	**−42**
Power, P_{DC} (mW)	65.9	36.6#	14.1	82.9	35.5	22.5	26.6
Active area (mm²)	0.19	0.39#	0.39	0.35	0.36	0.16	0.13
$FoM_{JIT}$$	**−248.7**	**−240.3**	**−243.9**	**−221.1**	**−235.7**	**−248.2**	**−252.3**
$FoM_{JIT,M}$^	**−273.8**	**−271.5**	**−271.0**	**−254.2**	**−265.0**	**−271.3**	**−275.5**

*Calculated from measurements #Only for the D-band chain

$FoM_{JIT} = 10\log((\sigma_{RMS}/1s)^2 \cdot (P_{DC}/1\ mW))$ (dB) $FoM_{JIT,M} = FoM_{JIT} - 10\log(f_{OUT}/f_{REF})$ (dB)

☺ **The proposed W/D-band frequency synthesizer achieved the lowst RMS jitter, while also providing a wide frequency tuning range of 11.8%**

Acknowledgement The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

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