IDEC Chip Design Contest

A Low-Reference-Spur and Low-Jitter D-Band PLL with Complementary Power-Gating Injection-Locked Frequency-Multiplier-Based Phase Detector

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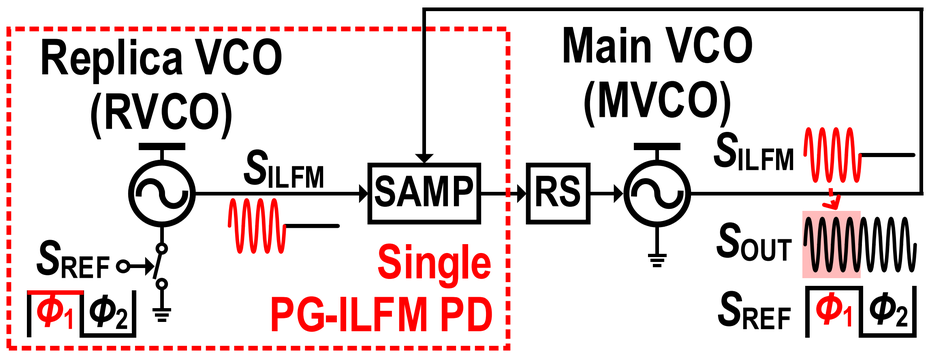
Problems of Prior Architecture

Conventional D-Band PLL using a Single Power-gating injection-locked-frequency-multiplier based PD



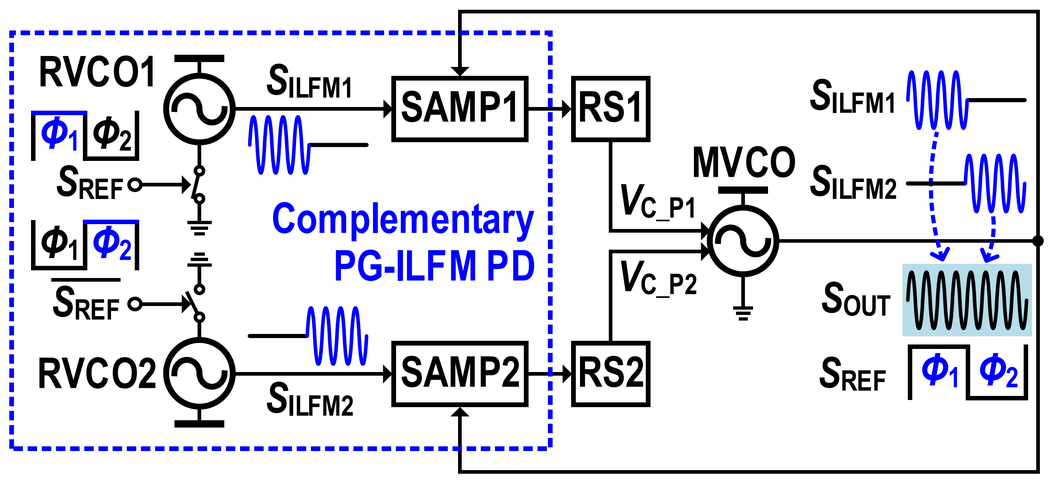
- Power-Gating Injection-Locked-Frequency-Multiplier PD (PG-ILFM PD) was recently introduced for high PD gain
- Generating high-frequency reference signal (S_{ILFM}) by turning the replica VCO (RVCO) on and off, it achieved high PD gain, But...

☹ BFSF modulation effect ➔ Increased reference spur

☹ Utilization of only half T_{REF} ➔ Increased jitter

Concept of Proposed Idea

Proposed W-Band PLL using Power-Gating ILFM-based PD

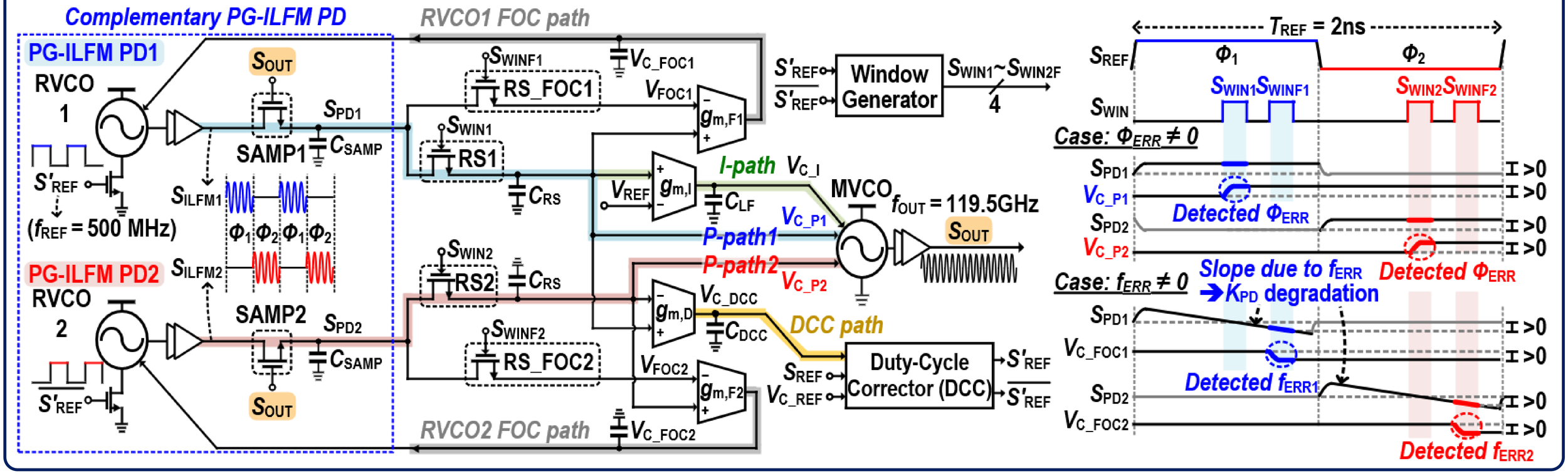


- Utilizing another PG-ILFMD PD2 for Φ_{ERR} detection

☺ No BFSK modulation effect ➔ Enhanced reference spur

☺ Utilization of whole TREF ➔ Decreased jitter

Architecture of Proposed D-Band PLL



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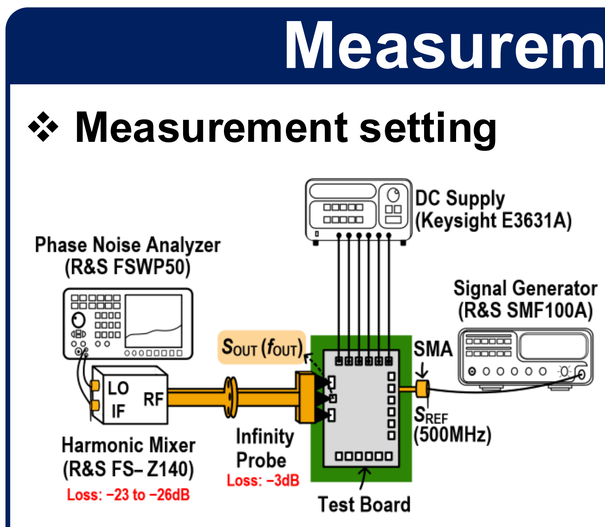
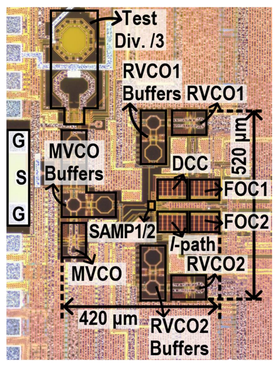
Measurement Results

❖ Measurement setting



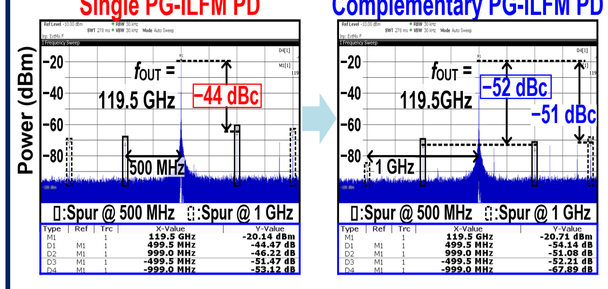
❖ Die photograph



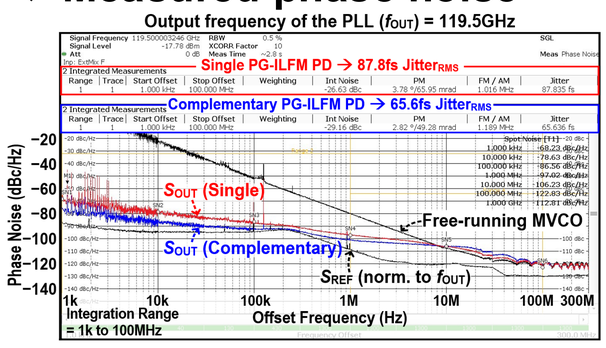
- ❖ 40-nm CMOS
- ❖ Active area: 0.22mm^2
- ❖ Power: 59.5mW

Power Consumption (mW)	
MVCO	18.0
RVCO1 & RVCO2	19.0
VCO buffers	18.0
SAMP1 & SAMP2 & *gm*-amplifier ($g_{m,I}$)	1.0
Window generator & FOCs & DCC	3.5
Total	59.5

❖ Measured spectrum



❖ Measured phase noise



☺ Achieving −51dBc reference spur and 65.6fs $Jitter_{RMS}$

Performance Comparison

	This work	ISSCC'21 [5]	ISSCC'23 [1]	VLSI'19 [2]	RFIC'14 [3]	JSSC'19 [4]	TMTT'16
Process (CMOS)	40nm	65nm	65nm	65nm	65nm	65nm	65nm
Architecture	**Direct PLL w/ Complementary PG-ILFM PD**	**Direct PLL w/ Single PG-ILFM PD**	**7.5GHz PLL + PLL (x18)**	**23GHz PLL + ILFM (x4)**	**50GHz PLL + Push-push (x2)**	**Direct ADPLL**	**61GHz PLL + Push-push (x2)**
f_{OUT} (GHz)	119.5	102.0	135.4	100.8	99.4	107.6	121.9
f_{REF} (MHz)	500	500	940	100	195	125	59.6
10MHz PN (dBc/Hz) Norm. to 120GHz	−106.2	−99.8	−102.3	−103.3	−103.4*	−103.1*	−102.6
$Jitter_{RMS}$, σ_{RMS} (fs)	66 (1k to 100M)	76* (1k to 100M)	87 (1k to 100M)	137 (10k to 10M)	170* (10k to 10M)	276 (10k to 10M)	959* (10k to 100M)
Ref. spur (dBc)	**−51**	**−42**	**−54**	**−33**	**−34***	**<−34**	**−30***
Power, P_{DC} (mW)	59.5	22.5	230**	23.6**	14.1	35.5	82.9
Active area (mm^2)	**0.27**	**0.16**	**0.84****	**0.41****	**0.39**	**0.36**	**0.35**
FoM_{JIT}*** (dB)	−245.9	−248.9	−237.6	−243.5	−243.9	−235.7	−221.2

*Calculated from measurements **Only for the W/D-band chain ***$FoM_{JIT} = 10\log[(\sigma_{RMS}/1s)^2 \cdot (P_{DC}/1mW)]$

☺ The proposed D-band PLL achieved the FOM_{JIT} of −245.9dB and −51dBc reference spur simultaneously, which can be applicable to radar, imaging, and cellular communications for 6G

Reference

[1] B. Moon et al., IEEE ISSCC, pp. 364-366, Feb. 2023. [2] X. Liu et al., IEEE RFIC, pp. 93-96, June 2014. [4] Z. Huang and H. C. Luong, IEEE JSSC, vol. 54, no. 2, pp. 358-367, Feb. 2019. [5] S. Yoo et al., IEEE ISSCC, pp. 330-331, Feb. 2021. [6] W. Wu et al., IEEE JSSC, vol. 54, no. 5, pp. 1254-1265, May 2019.

Acknowledgement

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