IDEC Chip Design Contest

A Low-Reference-Spur and Low-Jitter D-Band PLL with Complementary Power-Gating Injection-Locked Frequency-Multiplier-Based Phase Detector

Jaeho Kim¹, Jooeun Bang², Seohee Jung¹, Myeongho Han¹ and Jaehyouk Choi¹ ¹Seoul National University, Seoul, ²KAIST, Daejeon

Problems of Prior Architecture

Main VCO

Conventional D-Band PLL using a Single Power-gating injection-locked-frequency-multiplier based PD

Concept of Proposed Idea

Proposed W-Band PLL using Power-Gating ILFM-based PD





- Power-Gating Injection-Locked-Frequency-Multiplier PD (PG-**ILFM PD)** was recently introduced for high PD gain
- Generating high-frequency reference signal (S_{ILFM}) by turning the replica VCO (RVCO) on and off, it achieved high PD gain, But... ⊗ BFSF modulation effect → Increased reference spur \otimes Utilization of only half $T_{REF} \rightarrow$ Increased jitter
- Utilizing another PG-ILFMD PD2 for ϕ_{ERR} detection ◎ No BFSK modulation effect → Enhanced reference spur ☺ Utilization of whole TREF → Decreased jitter

Architecture of Proposed D-Band PLL



Measurement Results

Measurement setting



Die photograph

Div. /3

SAMP1/2

MVCO

RVC01



Performance Comparison

This work	ISSCC'21[5]	ISSCC'23[1]	VLSI'19[2]	RFIC'14[3]	JSSC'19[4]	TMTT'16	
40nm	65nm	65nm	65nm	65nm	65nm	65nm	
Direct PLL w/ Complementary PG-ILFM PD	Direct PLL w/ Single PG-ILFM PD	7.5GHz PLL + PLL (x18)	23GHz PLL + ILFM (x4)	50GHz PLL + Push- push (x2)	Direct ADPLL	61GHz PLL + Push- push (x2)	
119.5	102.0	135.4	100.8	99.4	107.6	121.9	
500	500	940	100	195	125	<mark>59.6</mark>	
-106.2	-99.8	-102.3	-103.3	-103.4*	-103.1*	-102.6	
66 (1k to 100M)	76* (1k to 100M)	87 (1k to 100M)	137 (10k to 10M)	170* (10k to 10M)	276 (10k to 10M)	959* (10k to 100M)	
-51	-42	-54	-33	-34*	<-34	-30*	
59.5	22.5	230**	23.6**	14.1	35.5	82.9	
0.27	0.16	0.84**	0.41**	0.39	0.36	0.35	
-245.9	-248.9	-237.6	-243.5	-243.9	-235.7	-221.2	
neasurements	**Only for t	he W/D-ban	d chain ***F	οM _{JIT} = 10lo	g[(σ _{RMS} /1s) ² ·	(P _{DC} /1mW)]	
The proposed D-band PLL achieved the FOM _{JIT} of -245.9dE							
and -51dBc reference spur simultaneously, which can be							
applicable to radar, imaging, and cellular communications for 6G							
	This work 40nm Direct PLL w/ Complementary PG-ILFM PD 119.5 500 -106.2 66 (1k to 100M) -51 59.5 0.27 -245.9 neasurements osed D-k c referents	This workISSCC'21[5]40nm65nmDirect PLL w/ Complementary PG-ILFM PDDirect PLL w/ Single PG-ILFM PD119.5102.0500500-106.2-99.866 (1k to 100M)76* (1k to 100M)-51-4259.522.50.270.16-245.9-248.9neasurements**Only for tCrefere Crefere Cradar, imaging	This work ISSCC'21[5] ISSCC'23[1] 40nm 65nm 65nm Direct PLL w/ Complementary PG-ILFM PD Direct PLL w/ Single PG-ILFM PD 7.5GHz PLL + PLL (x18) 119.5 102.0 135.4 500 500 940 -106.2 -99.8 -102.3 66 76* 87 (1k to 100M) (1k to 100M) (1k to 100M) -51 -42 -54 59.5 22.5 230** 0.27 0.16 0.84** -245.9 -248.9 -237.6 neasurements **Only for the W/D-band Osed D-band PLL achie Creference spur sime Creference spur sime Sime	This work ISSCC'21[5] ISSCC'23[1] VLSI'19[2] 40nm 65nm 65nm 65nm Direct PLL w/ Complementary PG-ILFM PD Direct PLL w/ Single PG-ILFM PD 7.5GHz PLL + PLL (x18) 23GHz PLL + ILFM (x4) 119.5 102.0 135.4 100.8 500 500 940 100 -106.2 -99.8 -102.3 -103.3 66 76* 87 137 (1k to 100M) (1k to 100M) (10k to 10M) -51 -42 -54 -33 59.5 22.5 230** 23.6** 0.27 0.16 0.84** 0.41** -245.9 -248.9 -237.6 -243.5 measurements **Only for the W/D-band chain ***F Osed D-band PLL achieved the chain ***F Osed D-band PLL achieved the chain ***F	This work ISSCC'21[5] ISSCC'23[1] VLSI'19[2] RFIC'14[3] 40nm 65nm 65nm 65nm 65nm Direct PLL w/ Complementary PG-ILFM PD Direct PLL w/ Single PG-ILFM PD 7.5GHz PLL t PLL (x18) 23GHz PLL t PLL (x18) 50GHz PLL t Push- push (x2) 119.5 102.0 135.4 100.8 99.4 500 500 940 100 195 -106.2 -99.8 -102.3 -103.3 -103.4* 66 76* 87 137 170* (1k to 100M) (1k to 100M) (10k to 10M) (10k to 10M) -51 -42 -54 -33 -34* 59.5 22.5 230** 23.6** 14.1 0.27 0.16 0.84** 0.41** 0.39 -245.9 -248.9 -237.6 -243.5 -243.9 neasurements **Only for the W/D-band chain ***FOMJIT = 10lo Osed D-band PLL achieved the FOM, creference spur simultaneously, 'value simulation of the simula	This work ISSCC'21 [5] ISSCC'23 [1] VLSI'19 [2] RFIC'14 [3] JSSC'19 [4] 40nm 65nm 65nm 65nm 65nm 65nm 65nm Direct PLL w/ Complementary PG-ILFM PD Direct PLL w/ Single PG-ILFM PD 7.5GHz PLL v/ Single PG-ILFM PD 23GHz PLL + PLL (x18) 50GHz PLL + Push- push (x2) Direct ADPLL 119.5 102.0 135.4 100.8 99.4 107.6 500 500 940 100 195 125 -106.2 -99.8 -102.3 -103.3 -103.4* -103.1* 66 76* 87 137 170* 276 (1k to 100M) (1k to 100M) (10k to 10M) (10k to 10M) (10k to 10M) (10k to 10M) -51 -42 -54 -33 -34* <-34 59.5 22.5 230** 23.6** 14.1 35.5 0.27 0.16 0.84** 0.41** 0.39 0.36 -245.9 -248.9 -237.6 -243.5 -243.9	



420 µm RVCO2	Window generato & FOCs & DCC
Buffers	Total
& Maacurad ph	aco noi

Measured spectrum





○ Achieving -51dBc reference spur and 65.6fs Jitter_{RMS}

Reference

[1] B. Moon et al., IEEE ISSCC, pp. 364-366, Feb. 2023. [2] X. Liu et al., IEEE RFIC, pp. 93-96, June 2014. [4] Z. Huang and H. C. Luong, IEEE JSSC, vol. 54, no. 2, pp. 358-367, Feb. 2019. [5] S. Yoo et al., IEEE ISSCC, pp. 330-331, Feb. 2021. [6] W. Wu et al., IEEE JSSC, vol. 54, no. 5, pp. 1254-1265, May 2019.

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