

# **Echo-canceling FFE Transmitter for Multi-Drop Bus**

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#### Introduction

#### Multi-drop Bus in Memory Interface

Provides an area, power efficient method to extend memory capacity.



- Overall Architecture of the transmitter
  - Datapath consists of PRBS generator, N-UI delay chain, main/EC taps, pre-driver and output driver.
  - Uses half-rate architecture, with 6GHz differential clocks' duty cycles corrected using duty cycle corrector (DCC)
  - EC tap delay  $\tau_d$  consists of  $t_{UI}$  and  $t_{VCDL}$ , which are implemented using N-UI delay chain and VCDL, respectively.

#### Characteristics of Multi-drop Bus

• Due to impedance discontinuities, multi-drop bus exhibits reflective inter-symbol-interference (ISI).

### Proposed Echo-canceling FFE Transmitter

- Echo-canceling (EC) pulse is transmitted  $\tau_d$  after the main pulse.
- The amplitude of  $\tau_{\text{d}}$  is adjusted to cancel reflection.
- With sufficient number of echo-canceling taps, reflective ISI can be removed.





#### Chip Photo and Simulation/Chip Results



#### Contributions and Scope of the Work

Remove reflective ISI in an MDB	Applicable for wide range of stubs
• Effectively removes reflective ISI in an MDB channel and delivers open-eye to RX.	<ul> <li>Unlike some of prior works, this work can be applied to short/long length stubs.</li> </ul>

## **Overall Architecture**

- Architecture of the proposed echo-canceling FFE transmitter
  - 6 EC taps for removing reflective ISI.
  - In each EC tap, 1-tap FFE is used to match EC pulse to the reflection.

Conceptual Architecture of the EC-FFE

Operation of Multi-tap EC with Pulse shaping

#### Implemented with Samsung 28nm CMOS Technology

- Achieves 0.29UI eye opening for 1E-12 BER at 12Gbps.
- EC-FFE and pulse shaping results in eye height of 30.6mV and eye width of 0.62UI at 12Gbps.







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With conventional FFE

EC-FFE, Pulse shaping disabled EC-FFE, Pulse shaping enabled

#### Acknowledgement

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