IDEC Chip Design Contest

Design of Physically Unclonable Function Operation Circuit without Using a Reference Based on NAND Flash Structure

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Introduction

PUF Circuit Design: Eliminates the need for a reference capacitor and voltage.
Disadvantages of Traditional PUF Design: Requires separate reference elements, leading to increased complexity and power consumption.
Randomness Source: Utilizes parasitic capacitors in NAND flash structure.
Challenge Input Capacity: Supports $2^{16}\times{}_{16}C_2$ combinations.

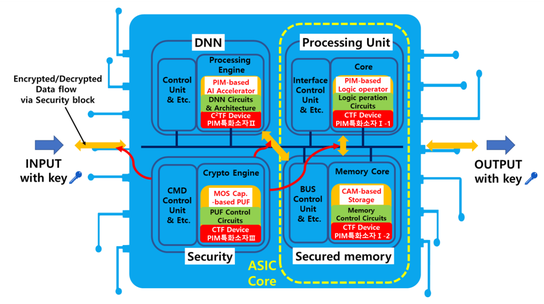


Fig. 1. A single chip integrating Boolean operations, associative memory, deep learning, and anti-counterfeiting

Circuit Design

❖Proposed circuit schematics

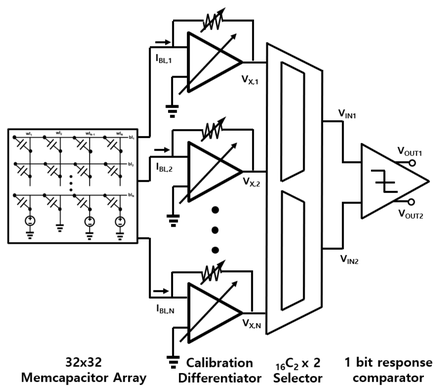


Fig. 2. The system of PUF operating circuit

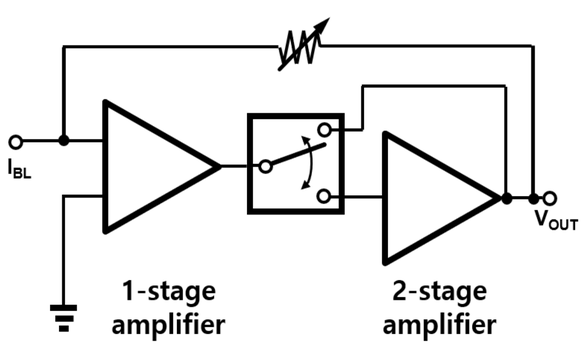


Fig. 3. The calibration differentiator

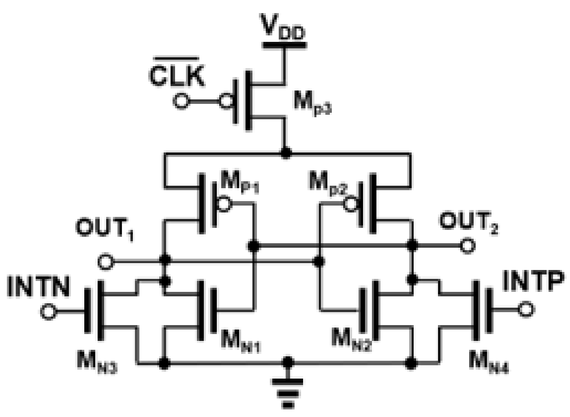


Fig. 4. The comparator

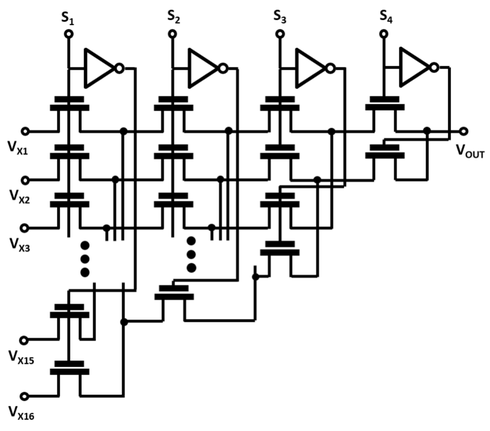
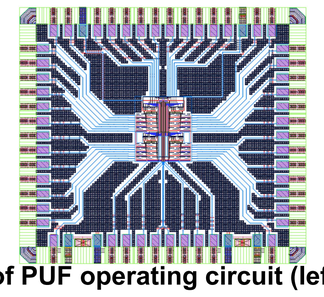


Fig. 5. The MUX of selector

◆Features of PUF operating circuit

- **In fig. 2, exploiting NAND flash parasitic capacitances and process variations, the circuit generates randomness without external reference signals.**
- **Word Line Selection and Input:** A 16×16 memory cell array is employed, where a single word line is driven from high (1) to low (0).
- **The calibration differentiator in fig. 3:** The differentiator detects these changes and converts the voltage drop over time into a differential signal.
- **The comparator in fig. 4:** These two signals then go to a sense amplifier, which compares their timing or voltage levels to produce a single-bit (‘0’ or ‘1’) response.
- **The MUX of selector in fig. 5:** Among the multiple signals from the differentiator, the selector picks two representative differential signals under certain conditions.
- **With a simple, energy-efficient design and excellent randomness, this PUF is well-suited for next-generation low-power, high-security applications.**

MPW Result



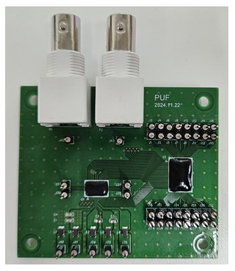


Fig. 6. Layout of PUF operating circuit (left side) and PCB of PUF operating circuit (right side)

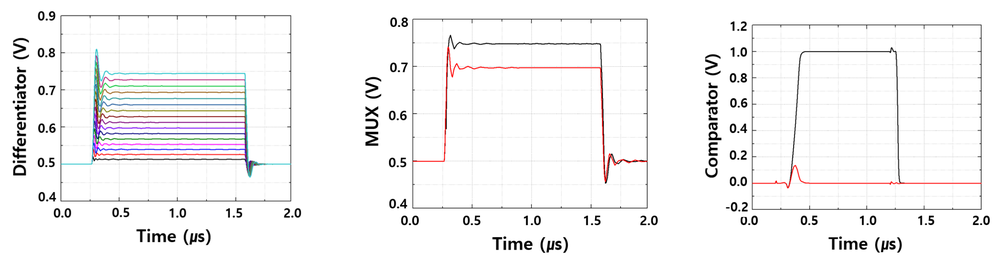


Fig. 7. (a) The transient simulation of differentiator, (b) the transient simulation of MUX (c) the transient simulation of comparator

◆Explanation of simulations and the chip

- **The layout and chip in fig. 6:** they shows the layout of the proposed circuit and the fabricated chip mounted on a PCB.
- **The simulation of differentiators in fig. 7(a):** it presents a simulation comparing the magnitudes of random capacitance differences.
- **The simulation of MUX in fig. 7(b):** it depicts a simulation in which two of those capacitance values are selected and their outputs are shown.
- **The simulation of comparator in fig. 7(c):** it illustrates a simulation where the MUX compares these two selected values to generate the final output.
- **The tables the specifications of the circuit, highlighting its low power consumption and high reliability.**

❖Tables of performances

Performance	Differentiator
Phase margin	72°
Loop Gain	39 dB
Power	36.7 uW

Performance	Comparator
Delay	117.1 ps
Power	84.6 uW
Input-Referred noise	435 uV/(Hz)$^{-1/2}$

Performance	PUF operation circuit
Energy Efficiency	472.7 pJ/bit
Diffuseness	50±1 %

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.