IDEC Chip Design Contest

DC to 50GHz SPDT switch in 28nm FD-SOI

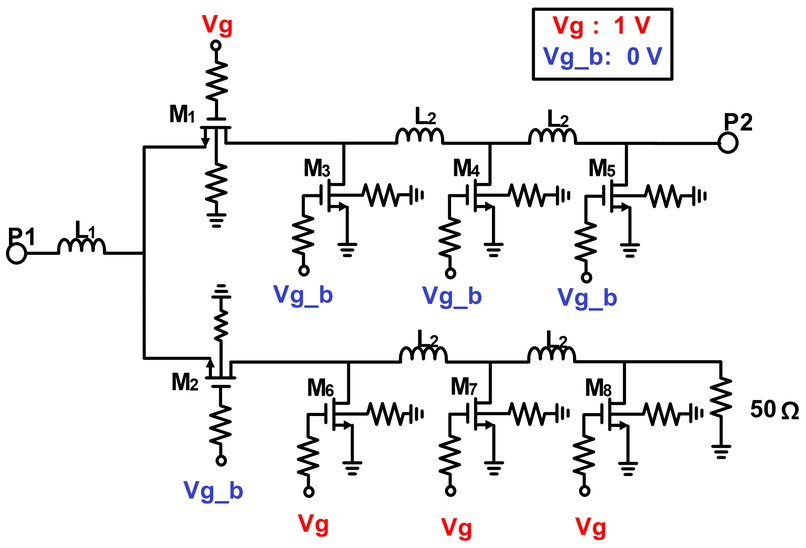
Sangmin Kim, Seungwoo Shim and Sanggeun Jeon
School of Electrical Engineering, Korea University, Seoul 136-713, Korea

Introduction

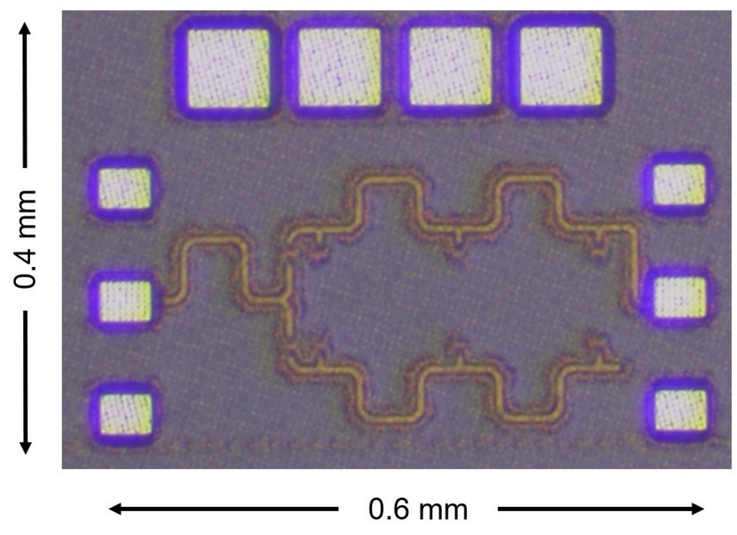
- **The necessity of single-pole double-throw (SPDT) switch**
  - Enables Tx/Rx path control with high isolation in multi-band,multi-mode RF systems.
  - Require low insertion loss to maintain transmitter efficiency and receiver noise figure.
- **Advantages of the FD-SOI**
  - Scalable technology with low leakage current, suitable for high-frequency, low-power applications.
  - Ultra-thin BOX layer provides excellent substrate isolation and minimizes parasitic coupling.

Design

- Series-shunt topology enables high isolation.
- A three-stage shunt transistor structure enables wideband operation with low insertion loss and high isolation.
- Layout optimized to achieve DC-50 GHz operation with compact footprint
- Chip size : 0.6 x 0.4 mm^2.



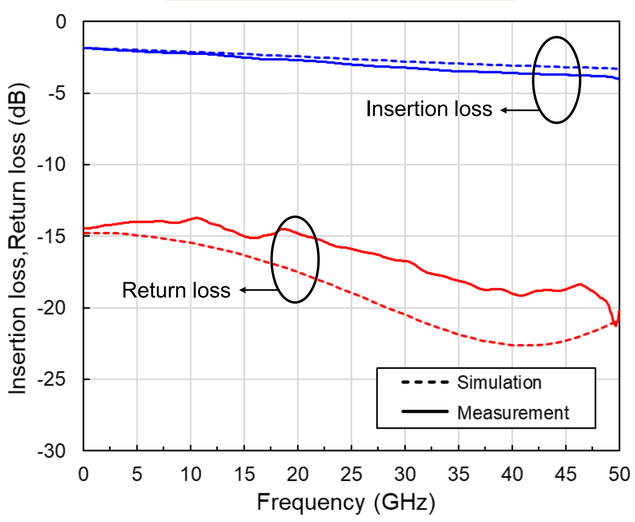
SPDT Schematic



SPDT Chip micrograph

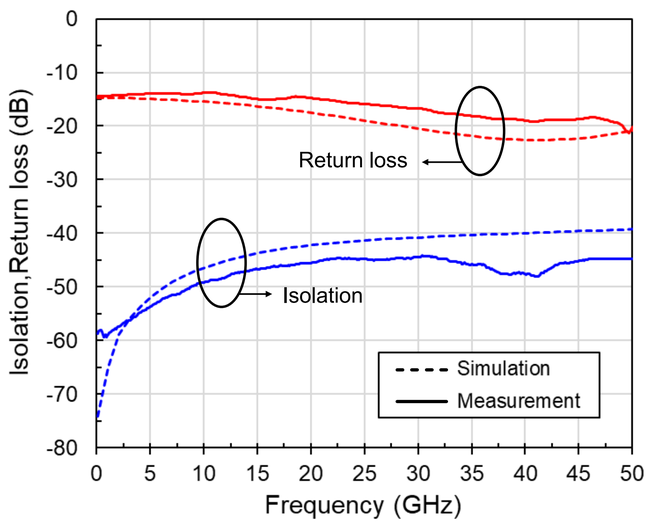
Measurement Results

ON-state



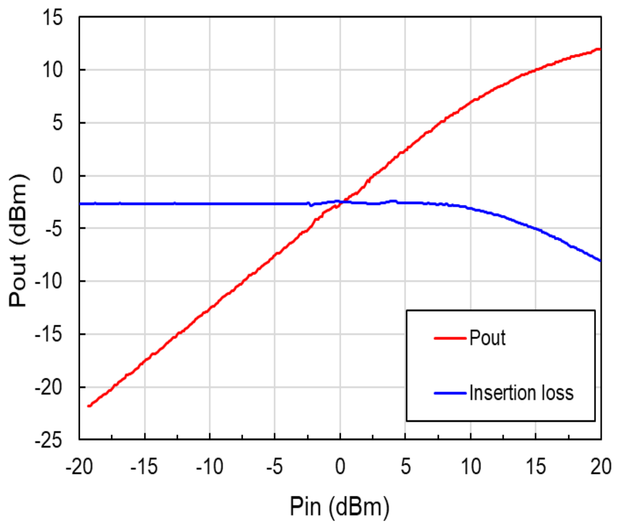
- Insertion loss : 1.85 - 4.02 dB
- Return loss : 14.4 - 20.2 dB

OFF-state



- Isolation : 44.7 – 58.7 dB
- Return loss : 14.4 - 20.2 dB

P_{1dB}



- P_{1dB} : 11.5 dBm @ 20GHz

Conclusion

- We have developed a DC to 50 GHz SPDT switch in a 28-nm FD-SOI process.
- The switch achieves an insertion loss of 1.85–4.02 dB and an isolation of 44.7–58.7 dB across the operating band.

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