

Low-Power Edge Detection Algorithm for Retinal

Prostheses

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Introduction

This study introduces a low-power edge detection algorithm designed for retinal implants. It is implemented on a 256-pixel chip using a SB 130 nm BCDMOS process, which allows precise analog control and easy integration. As more pixels are packed into a small area, current can leak between pixels and generate heat. Existing methods often turn on too many pixels, which leads to high power use and slower processing. The proposed RPED algorithm reduces the number of active pixels but still keeps important image edges clear. Simulations show that the chip works reliably with low power, making it suitable for compact retinal implants.



Block Schematic Architecture

Experimental Results

The retinal pixel-edge detection (RPED) algorithm is implemented in a retinal implant to reduce power consumption while preserving critical visual details by stimulating only the pixels corresponding to detected edges. Unlike conventional full-frame stimulation, which would activate all pixels simultaneously, the RPED method compares neighboring pixel intensities and activates only two adjacent pixels per comparison event(Fig. 1(a, b)). In operation, incoming light is first sensed by a photodiode, which triggers an initial pair of target pixels; the algorithm then proceeds sequentially through the pixel array, comparing adjacent pixels to detect edges(Fig. 1(c)). The RPED logic counts the resulting pulses from each pixel to determine its intensity. The light-intensity-dependent pulse signal is generated through an analog circuit. A photodiode-based pulsefrequency modulation (PFM) senses the incoming light intensity and converts it into a digital pulse train. We employs a source-follower circuit to overcome the speed limitations (Fig. 1(d)). A current-driver circuit processes the pulse train using a beta-multiplier reference and a push-pull output stage to generate alternating anodic and cathodic current pulses that are delivered to the corresponding retinal electrodes(Fig. 1(e)). Proposed algorithm system enables pixel-level stimulation with reduced power usage. Figure 2 presents pixel-level stimulation pulse train and Figure 4 shows experimental results demonstrating the performance of the implemented RPED algorithm.







(b)

Figure 3. (a) A microscopic image of the retina chip (b) A demonstration bench for the proposed retina chip,

(a)







(c)

Figure 2. Observed transient output waveforms at each block. (a) The incoming light generates only five pulses. (b, c) Strong light generates over 16 PFM pulses during enable-high, prompting the controller to disable PFM and serialize 4-bit counter data into pulses. (b) If the pulse count is not a multiple of 16 when enable is low, the system behaves like in the weak light condition. (c) When the number of PFM pulses is a multiple of 16, the enable signal goes low, but serialization of the counter data continues regardless of the enable state.

Figure 4. Image results of (a) traditional light intensity stimulation and (b) edge detection stimulation applying RPED algorithm using the retinal prosthesis 256-pixel stimulation chip

Conclusion

We developed and tested the RPED algorithm to improve image clarity while using less power. It was verified through MATLAB simulations and tested on a 256-pixel retinal stimulator made with the SB130 BCDMOS process. The algorithm showed better performance than the conventional method, with a PSNR of 8.86 and an SSIM of 0.34. Power use was reduced to 37.5 mW, which is 25 mW lower than traditional methods. By activating only edge-related pixels, the algorithm cuts power and lowers the risk of heat damage. We plan to apply RPED to a 2000-pixel retinal chip now under development.

Figure 1. (a) Stimulation methods of {a} light intensity {b} edge extraction. (b) Comparison of the principle between conventional edge detection stimulation (blue) and RPED algorithm stimulation (red). (c) Flow chart of the proposed RPED algorithm. (d) Proposed pulse frequency modulation circuit diagram (e) Push–pull structure-based biphasic current driver circuit

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