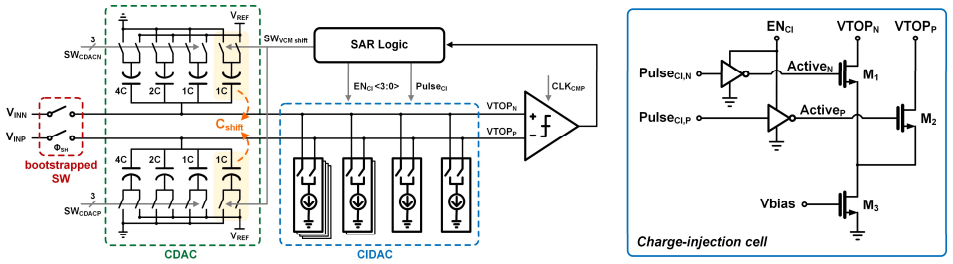
IDEC Chip Design Contest

A 7-bit 17-fJ/conv-step Area-Efficient asynchronous C-CIDAC SAR ADC

Junmin Park and Hyungil Chae
Konkuk University

- The speed of digital processing by hardware is constantly increasing due to technology scaling, and the demand for high-speed ADCs is also increasing
- In the design of Time-interleaving, which is an essential technology for high-speed ADCs, small area and low power consumption of a single slice ADC become critical goals
- This work proposes an improved hybrid structure of C-CIDAC SAR ADC

Proposed C-CIDAC SAR ADC structure and CI cell



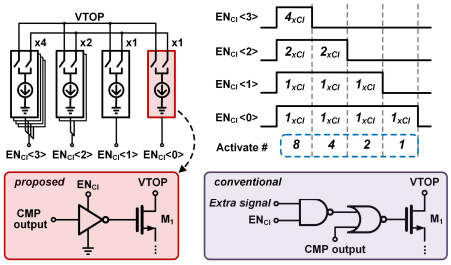
Improved hybrid structure of C-CIDAC SAR ADC

- MSB conversion : **CDAC** & LSB conversion : **CIDAC**
  - ✓ Decrease overall area and design complexity
  - ✓ Utilize CIDAC for LSB conversion with a low linearity requirement
- CDAC 3bits + CIDAC 4bits
  - ✓ Optimize the trade-off between area and linearity
  - ✓ One bit of redundancy corresponding to the LSB size of the CDAC to tolerate the decision error and stage gain mismatch

Charge-injection cell (CI cell)

- M_1 & M_2 : Switch the discharge direction
- M_3 : Determines the discharge amount
- Minimize the digital logic and number of transistors
  - ✓ The CIDAC area greatly reduces

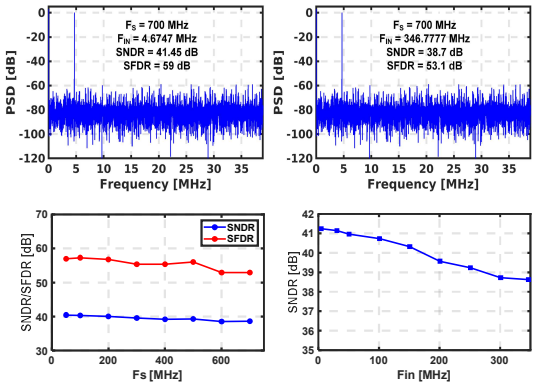
CI Pulse gating



Power gating

- Reusing CI cells increases digital logic complexity
  - → affecting the power consumption and area
- New pulse gating scheme
  - ✓ Turn on/off the Inverter supply voltage
  - ✓ Minimum logic gate delay to CI cell
    - → simplify digital logic and CI cell
    - → helpful in terms of power consumption and area

Measurement Results



- Process : 28nm CMOS
- Supply voltage : 0.9V
- Active area : 259um^2
- (top) : Measured power spectral density
  - ✓ Maximum SNDR : 41.45dB / 38.7dB
  - ✓ Maximum SFDR : 59dB / 53.1dB
- (bottom left) : SNDR and SFDR vs Sampling frequency
- (bottom right) : SNDR vs Input frequency

Comparison table and Performance comparison

	This Work	ASSCC'24	ASSCC'23	CICC'23	ISSCC'16	JSSC'20
Architecture	**C-CI SAR**	CI-C SAR	C-CI-CI SAR	CI SAR	CI SAR	SAR FLASH
Technology [nm]	**28**	28	28	28	40	28
Supply [V]	**0.9**	0.9	1	0.95	1	1.1
Fs [GS/s]	**0.7**	0.6	1	1.1	1	1
Resolution [bits]	**7**	8	8	6	6	8
SNDR [dB]	**38.7**	43.5	43.5	35.2	35.1	45.5
SFDR [dB]	**53.1**	59.6	54.1	49.4	49.7	59.4
Power [mW]	**0.835**	1.48	2.61	1.32	1.26	2.55
Area [um^2]	**259**	848	261	226	580	5600
FoM_W [fJ/conv-step]	**17.03**	20.2	21.3	25.5	28.7	16.6

- Comparison table with other medium-resolution SAR ADCs using the CI scheme.
  - ✓ 7-bit C-CI SAR ADC at a sampling frequency of 700MHz
  - ✓ Achieves the best FoM_W of 17.03 fJ/conv-step
  - ✓ Achieves 0.835mW power consumption
  - ✓ Achieves Competitive area efficiency of 259um^2 area

- ✓ An improved hybrid structure of C-CIDAC SAR ADC with 7-bit resolution at a 700MHz sampling speed
- ✓ Achieves high area efficiency with good linearity by analyzing DAC stage configuration and bit allocation, as well as Pulse gating method
- ✓ Achieves a very small area and best FoM_W among the CI-based SAR ADCs, which is suitable to be used as a slice ADC for high-speed TI ADC

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.