IDEC Chip Design Contest

High-Speed SAR ADC for Wireline RX

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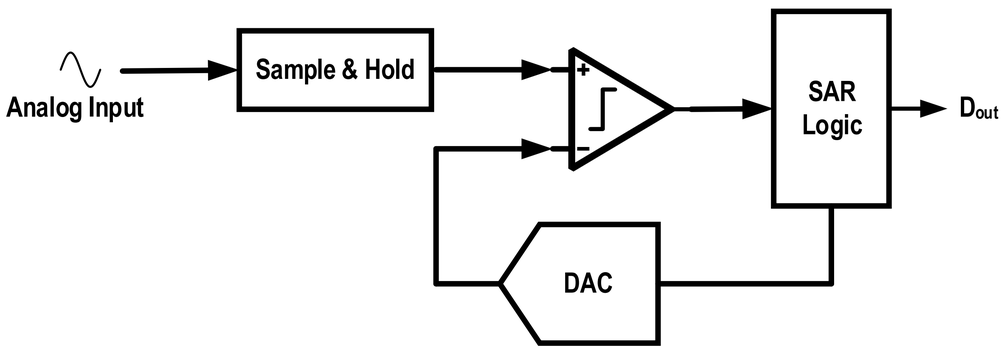
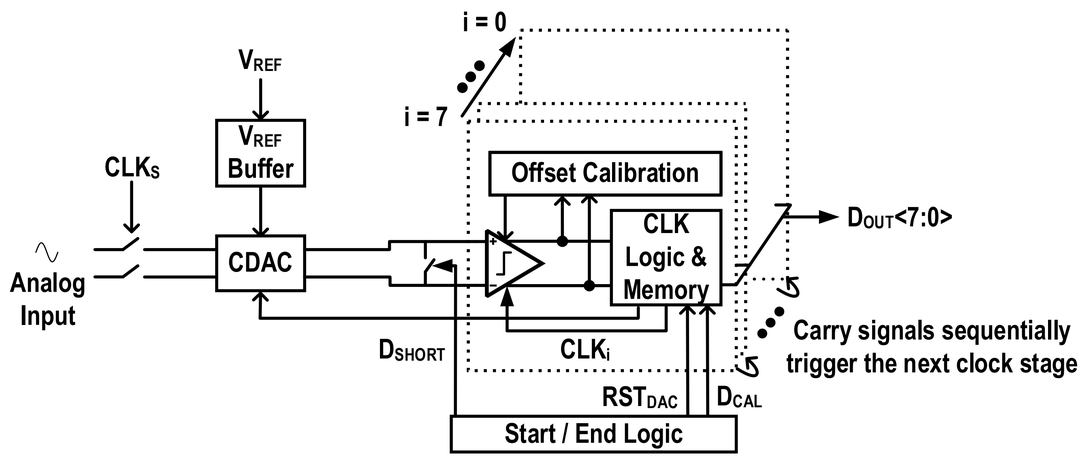
Introduction



<SAR ADC Block Diagram>

•SAR ADCs are widely used in high-speed wireline receivers for their simplicity and scalability.
•Their architectural simplicity enables high-speed operation with minimal power and area, making them ideal for wireline receivers.
•In particular, asynchronous timing and loop-unrolled structures have been explored to further enhance sampling rate and scalability.

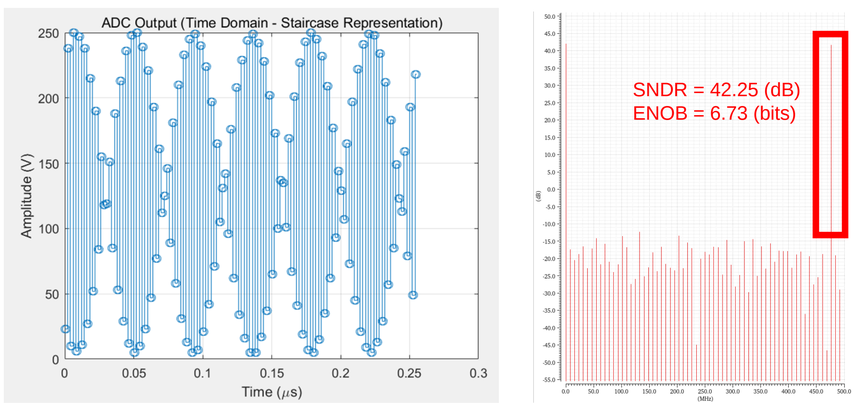
Architecture



<Loop-Unrolled Architecture>

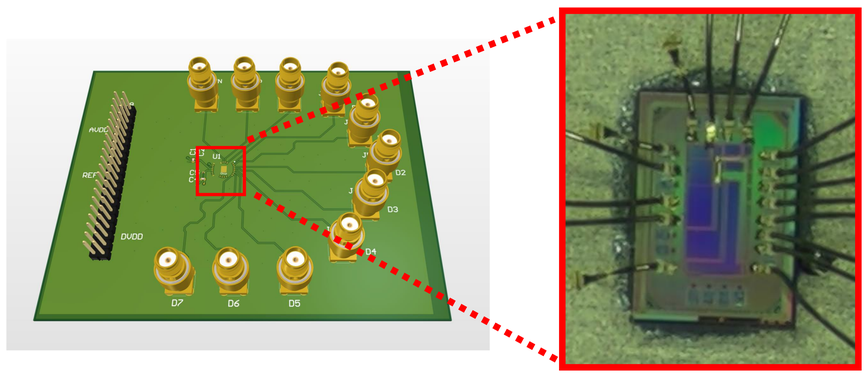
•8-stage loop-unrolled SAR ADC with asynchronous stage-by-stage triggering.
•Each stage includes a comparator, offset calibration, and local clock logic.
•This allows each stage to operate without waiting for a global clock.
•As a result, the ADC can run faster and more efficiently.

Results



<Post Simulation Results>

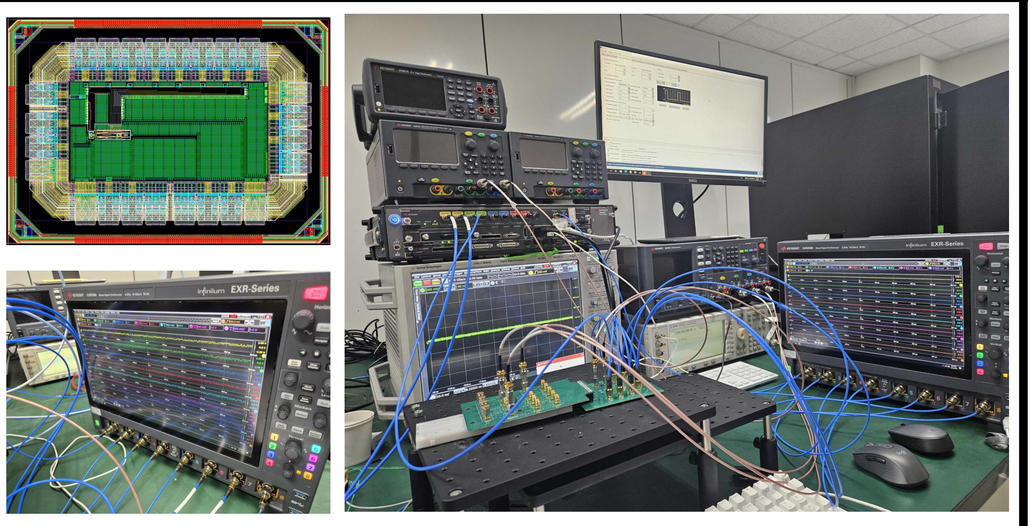
•Post-layout simulations indicate SNDR of 42.25 dB and ENOB of 6.73 bits at Nyquist input.



<PCB Implementation>

•A custom PCB was designed and wirebonded for chip testing.
•Power, reference, input, and digital I/O are accessible via SMA and pin headers.

Chip Layout & Measurement



•Measurement setup uses an 8-channel oscilloscope to capture all 8-bit digital outputs.
•Power, clock, and analog inputs are externally supplied via PCB.

Conclusion

•An 8-bit asynchronous SAR ADC was designed and fabricated in 28nm CMOS.
•The design adopts loop-unrolling to enable high-speed, stage-wise operation.
•Post-layout results show 42.25 dB SNDR and 6.73-bit ENOB at Nyquist input.
•Measurement confirms correct operation using PCB and oscilloscope setup.