IDEC Chip Design Contest

A Power-Efficiency 8-bit 2-GS/s Asynchronous Pseudo Loop-Unrolled SAR ADC

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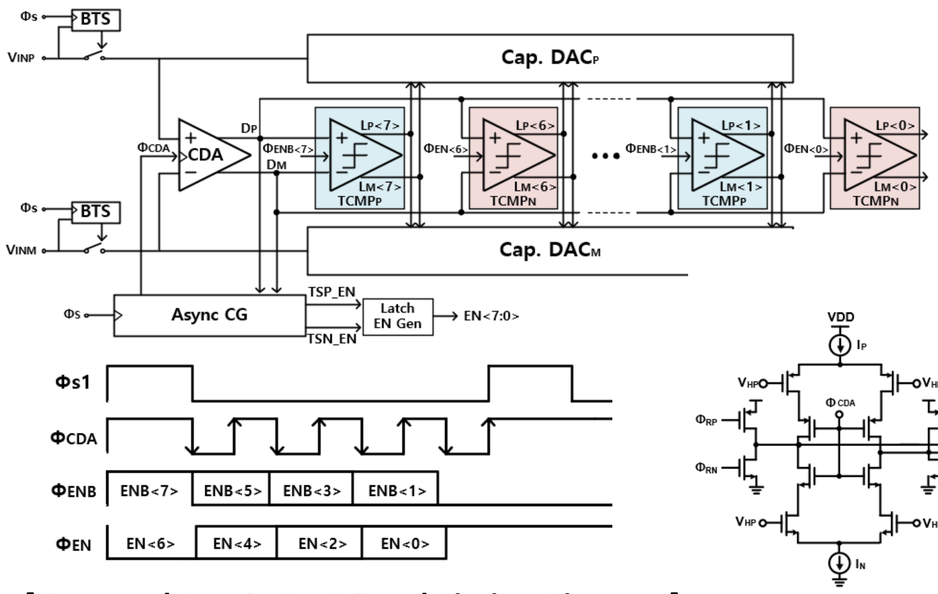
Introduction

➢ **Asynchronous Pseudo Loop-Unrolled SAR ADC**
- ✓ Only one CDA for preamplifier → Reduce offset calibration burden
- ✓ Loop-unrolled conversion → Eliminate register delay
- ✓ Self-triggered CDA's async. clock → Eliminate external high-speed clock

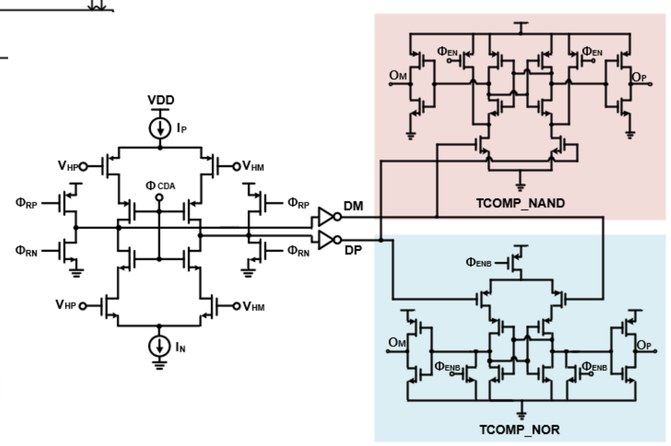
➔ **Faster conversion than conventional SAR ADCs**

➢ **Complementary Dynamic Amplifier (CDA)**
- ✓ Current reuse
- ✓ Twice conversion during one CLK period
- ✓ Reduce CLK driver & power consumption
- ✓ Generate Async. clock that are not metastable

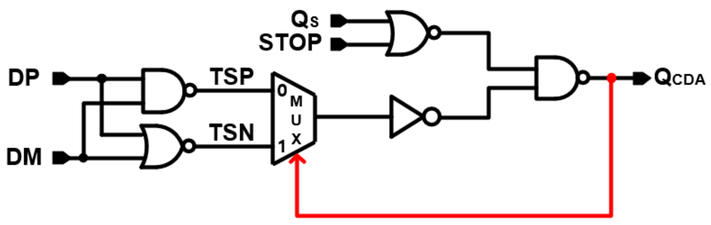
Proposed Asynchronous Pseudo Loop-Unrolled SAR ADC



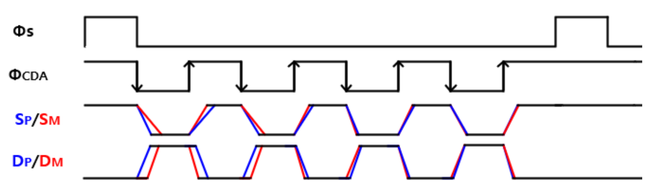
[Proposed PLU SAR ADC and Timing Diagram]



[CDA and TCOMP Circuit]

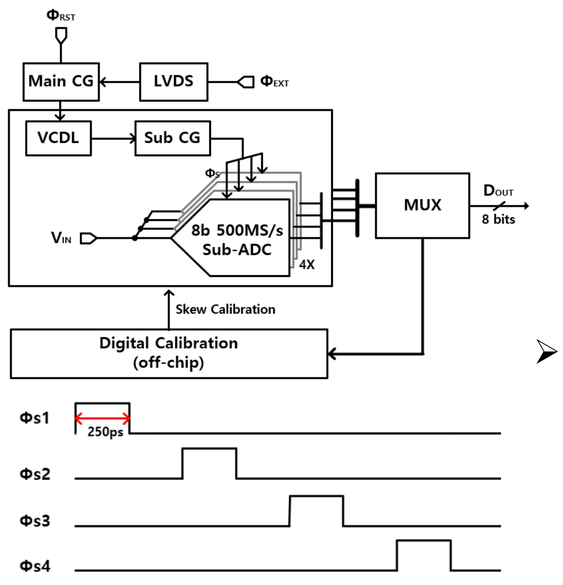


[Async CG MUX logic]



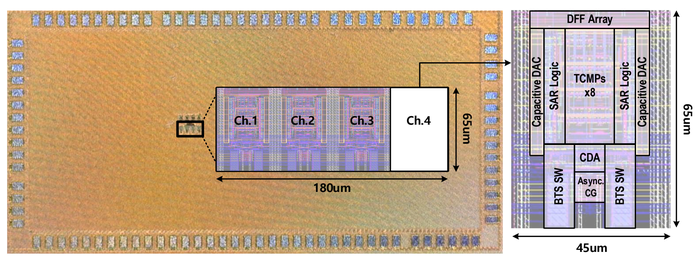
[CDA Timing Diagram]

➢ **Complementary Dynamic Amplifier (CDA)**
- ✓ CDA does not require a reset operation while conventional DA requires the reset operation.
- ✓ CDA's operating clock is generated by synchronizing to the dynamic output signals of the CDA, not the output signal of a time comparator that can be metastable.

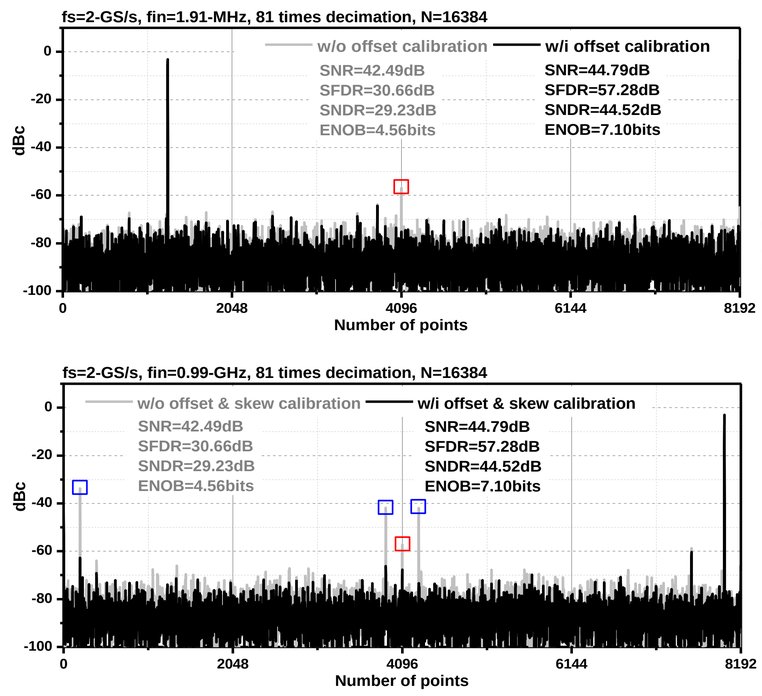


[4ch TI PLU SAR ADC block & timing diagram]

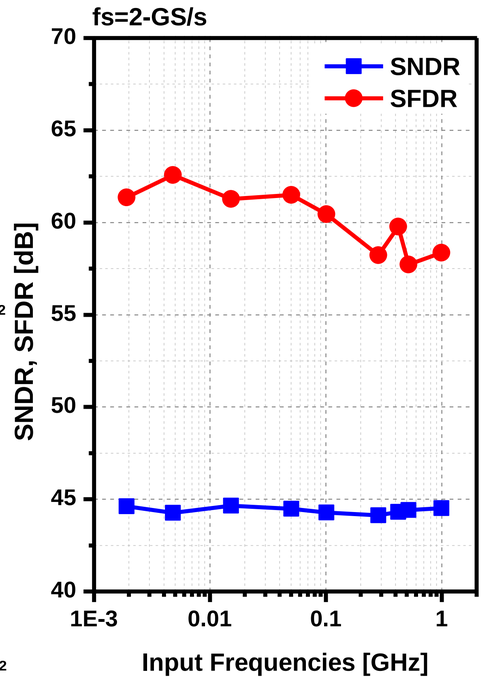
➢ **4-Channels Time-Interleaved SAR ADC**
- ✓ 8-bit 2-GS/s A-to-D conversion
- ✓ Channel mismatches
  - Offset: on-chip foreground calibration
  - Gain: no need
  - Time skew: off-chip digital calibration (VCDL)



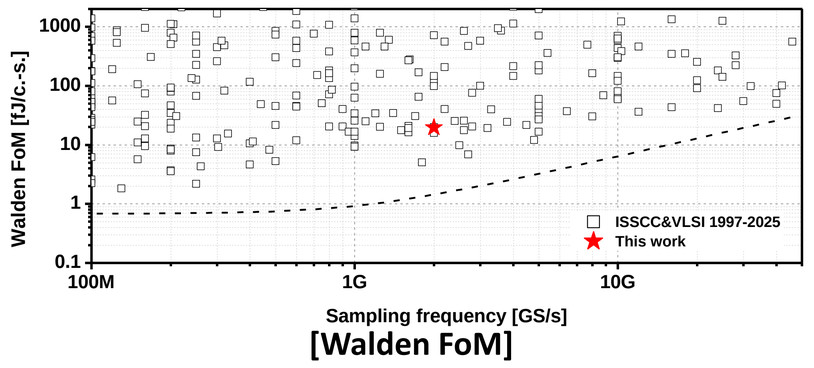
[Chip photograph]



[Measured FFT spectra at 2-GS/s]



[Measured SNDR and SFDR]



[Walden FoM]

	JSSC 18' S. Zhu	JSSC 17' H. Huang	VLSI 18' H. Chen	VLSI 20' D.-R. Oh	JSSC 18' C.-H. Chan	TCAS-I 21' W. Jiang	This work
Technology [nm]	65	65	40	28	28	28	**28**
# of channels	Single				2-ch. TI	4-ch. TI	**4-ch. TI**
Architecture	RNS TD	2-step SAR	2-step SAR	SAR-Flash	Multi-bit SAR	SAR	**P-LU SAR**
Supply [V]	1.2/1.3	1.25	1.2	1.1	0.9	1.2/0.9	**1.1**
Resolution [bit]	8	8	8	8	7	7	**8**
f_S [GS/s]	2.0	1.2	1.1	1.0	2.4	2.0	**2.0**
C_{INPUT} [fF]	128	45.5	Unknown	64	64	Unknown	**80**
Core area [mm²]	0.08	0.013	0.00165	0.002	0.0043	0.0082	**0.012**
Power [mW]	21	5.0	4.0	2.55	5.0	7.62	**5.4**
$ENOB_{@Nyq.}$ [bit]	6.5	6.96	7.18	7.26	6.36	5.75	**7.1**
FOM_{Walden} [fJ/c-s]	119	35	25.0	16.6	25.3	70.8	**19.6**

[Performance comparison table]

Measurement Results: Compared to previously reported 7~8-bit ADCs, it achieves high-speed, low-power performance at 7.1-bit ENOB.

Conclusion

- CDA-based asynchronous SAR conversion
- Power efficient CDA
- 8-bit 2-GS/s 44.52dB SNDR (7.1 ENOB) and 57.28dB SFDR

Acknowledgement

- The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.