IDEC Chip Design Contest

Domain-Specific SoC Prototype Featuring RISC-V CPU and CGRA with Host-Accessible Interface

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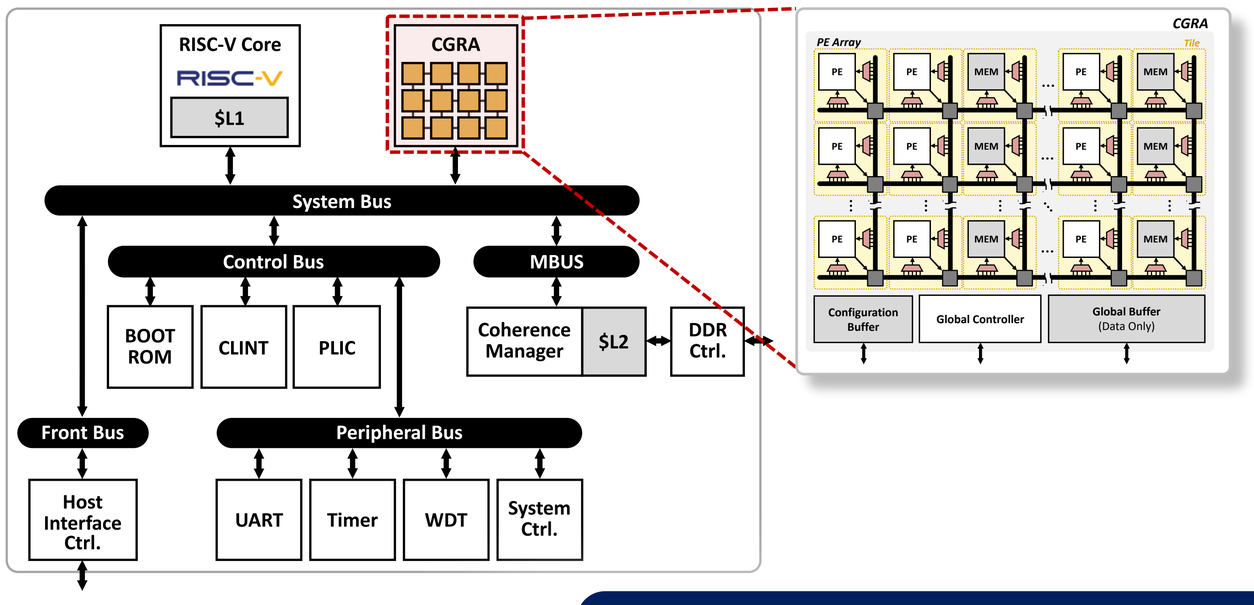
Introduction and Motivation

The rapid evolution of application domains such as AI, signal processing, and edge computing demands high-performance yet energy-efficient computing platforms. We present a SoC platform that integrates a RISC-V CPU with a Coarse-Grained Reconfigurable Array (CGRA), offering an open, flexible, and energy-efficient solution for domain-specific computing. The RISC-V core provides a lightweight and extensible ISA foundation, while the CGRA accelerates parallel and compute-intensive workloads common in AI, signal processing, and edge applications. To support efficient development and verification, the SoC includes a Host Interface that enables external control and observation, facilitating real-time debugging and rapid prototyping.

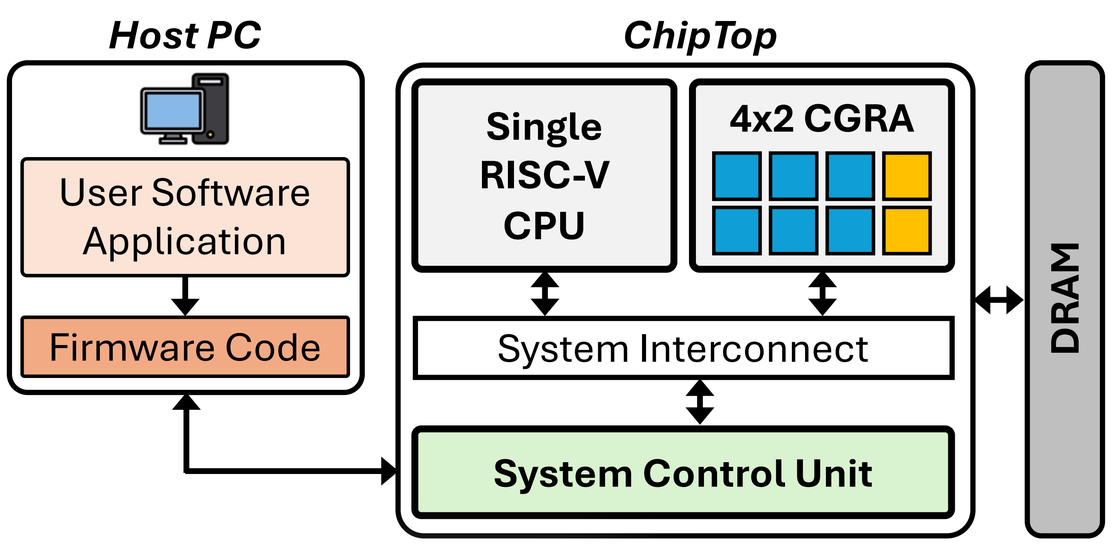
Overall Architecture

- Single **RISC-V core**
- **CGRA** for computation acceleration
- **Host interface** for communication with an external PC
- Other peripherals



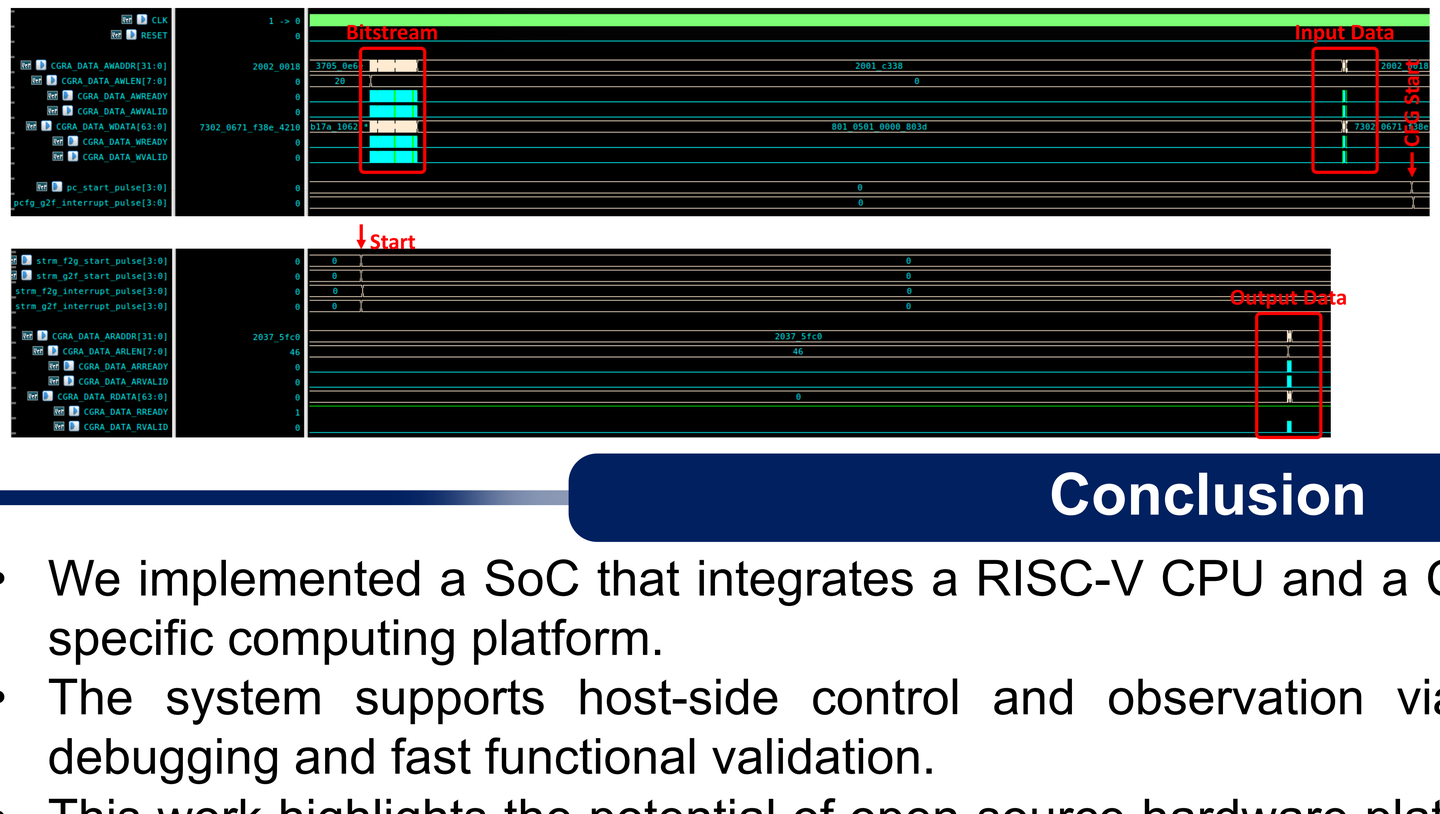
Method

- SoC reset and test program upload via host PC
- Test program (run on RISC-V core)
  - perform data/control for CGRA performance measurement



Result

- CGRA Result



Technology	TSMC 180nm
Core Voltage	1.8V
Max. Operating Frequency	50MHz
Circuit Type	Digital (Cell-based) Design
Core Size	5mm x 5mm
Verification	FPGA Proven

Conclusion

- We implemented a SoC that integrates a RISC-V CPU and a CGRA, demonstrating a flexible and domain-specific computing platform.
- The system supports host-side control and observation via a dedicated interface, enabling efficient debugging and fast functional validation.
- This work highlights the potential of open-source hardware platforms for rapid prototyping and innovation in AI, edge computing, and research-oriented applications.

Acknowledgement

This chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.