IDEC Chip Design Contest

Energy-Efficient Hybrid Spin-CMOS Logic Design Based on Cascadable Spin-Torque Majority Gate

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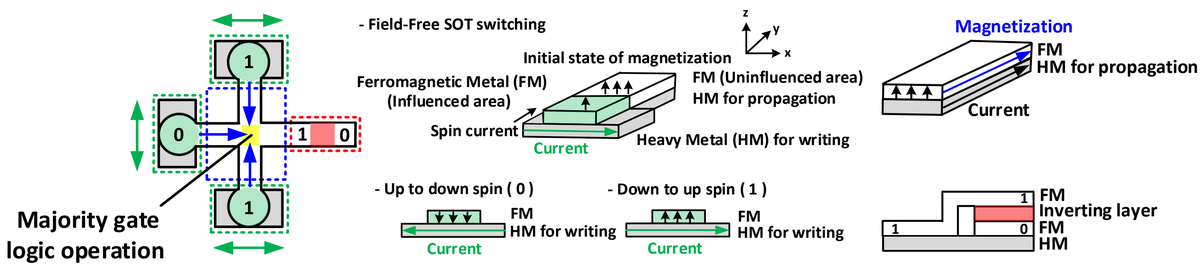
Introduction

STMG-based Logic

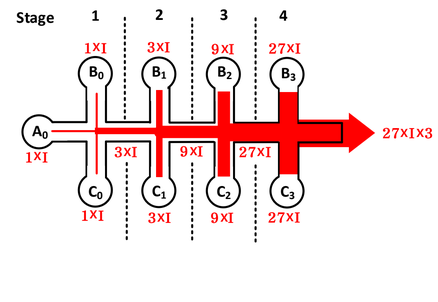
- Single device reconfigurable as AND / OR / NAND / NOR via mode-select input
- Near-zero leakage, nonvolatile, CMOS-compatible

Challenges in conventional STMGs

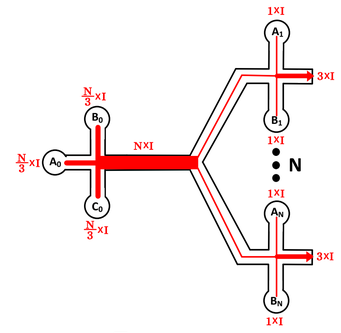
- **Cascading**: simultaneous operation across all stages → current grows 81× at stage 4 → FM breakdown
- **Fan-out**: N fan-outs require N×I current → FM breakdown



<Component of STMG>



<Cascading>

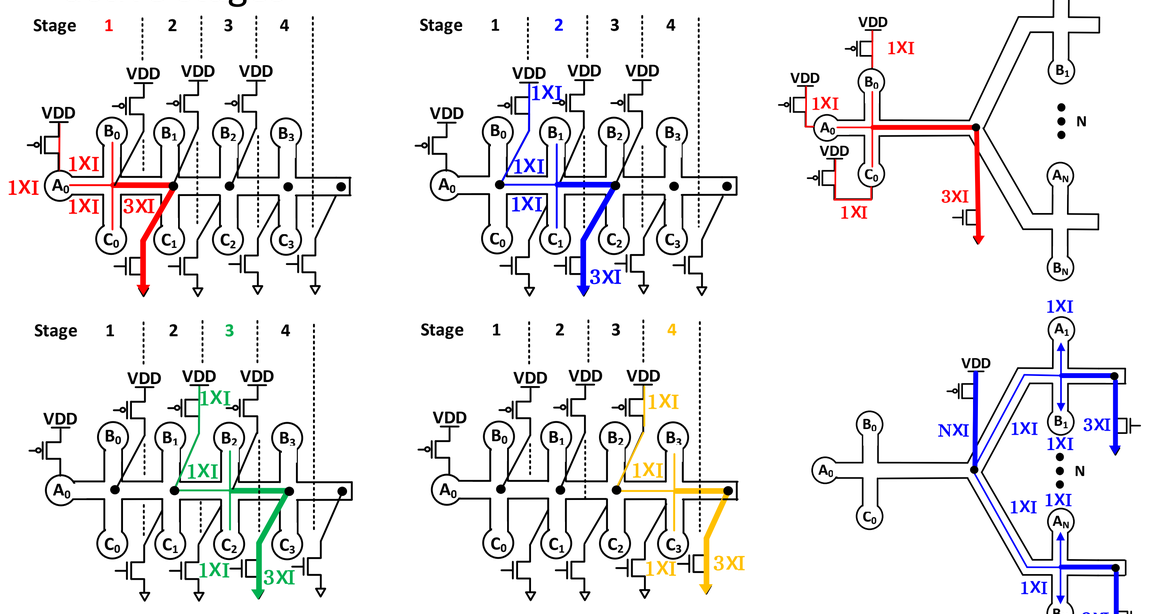


<Fan-out>

C-STMG

C-STMG = STMG device + clock-controlled transistors

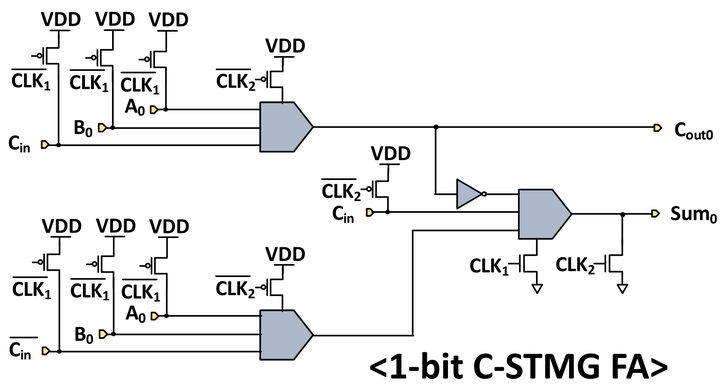
- Only selected stages activate per clock cycle → current always controlled to I
- Fan-out resolved: output = 3×I, input domain walls = I (independently sized per stage)
- Fine-grained pipelining → higher throughput, power only to active stages



<C-STMG Cascading> <C-STMG Fan-out>

1-bit FA Architecture:

- 3 C-STMGs, 2 clock stages (CLK_1 → stage 1, CLK_2 → stage 2)

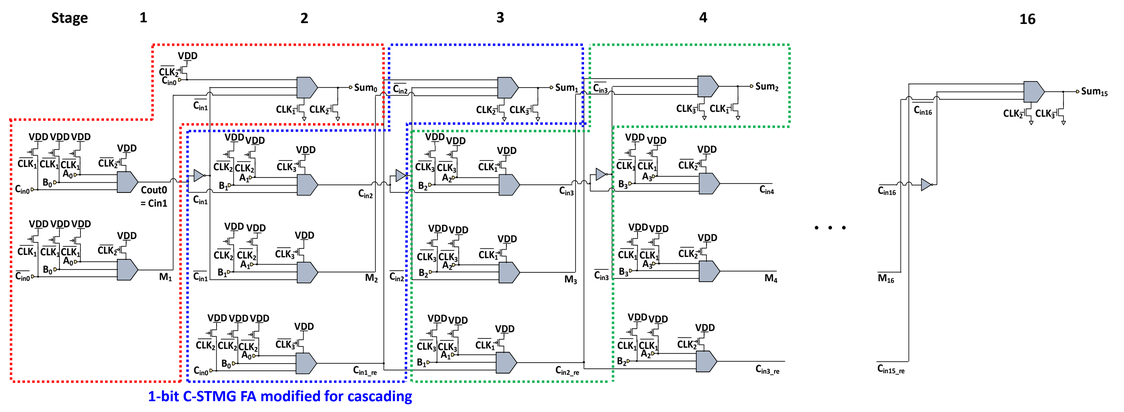


<1-bit C-STMG FA>

C-STMG Array

16/32/64-bit FA Array:

- 3 clock signals, clock duty = 1.1 ns (propagation: 0.89 ns, switching: 1.02 ns)
- Constant throughput at any bit-width via fine-grained pipelining

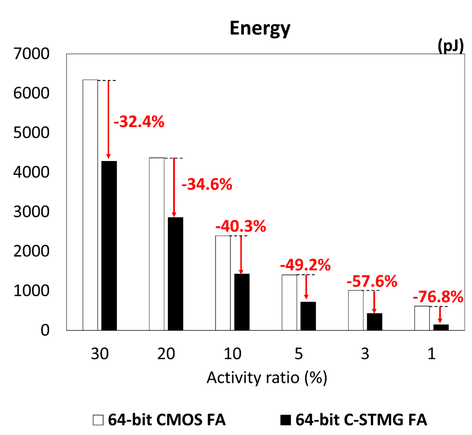


<16-bit C-STMG FA circuit>

Simulation & Result

- ≥28% lower energy vs CMOS across all bit-widths
- 76.8% energy reduction at 1% activity ratio (64-bit)

	Bit	CMOS FA	C-STMG FA
Delay – Throughput (ps)	16	380	3375
	32	690	3375
	64	1400	3375
Dynamic Power (µW)	16	3737	296
	32	4028	589
	64	4000	1175
Leakage Power (µW)	16	21.2	0
	32	41.5	0
	64	82.7	0
Number of Devices (TR : transistor)	16	1776	63 STMG 177 TR
	32	3504	127 STMG 353 TR
	64	6960	255 STMG 705 TR



Conclusion

- C-STMG resolves cascading & fan-out issues via sequential, clock-gated stage activation
- Constant throughput regardless of bit-width, zero leakage power
- 64-bit C-STMG FA: 76.8% lower energy at activity ratio vs CMOS FA

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The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), South Korea.