IDEC Chip Design Contest

Magnetically-AC-Coupled Voltage-Stacked Power Delivery

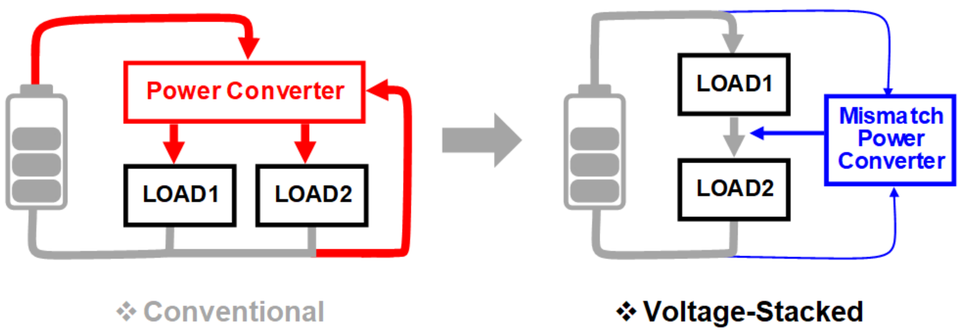
Seoyeong Yang[1] and SeongHwan Cho[1]
[1]KAIST, Daejeon, Korea

Introduction

Due to the increasing trend of supply current in semiconductor systems, conduction loss and voltage drop in the supply path have emerged as major issues. To mitigate these problems, a voltage-stack power delivery structure has been proposed, which delivers power at high voltage and low current by stacking loads in the voltage domain. This study proposes a magnetic AC-coupling based power management circuit to achieve the voltage-stack power delivery structure with high efficiency and high power density. We aimed at 82% converter efficiency under maximum power delivery and 0.11 A/mm^2 peak system current area density under 5MHz switching frequency in 3-stack power delivery system.

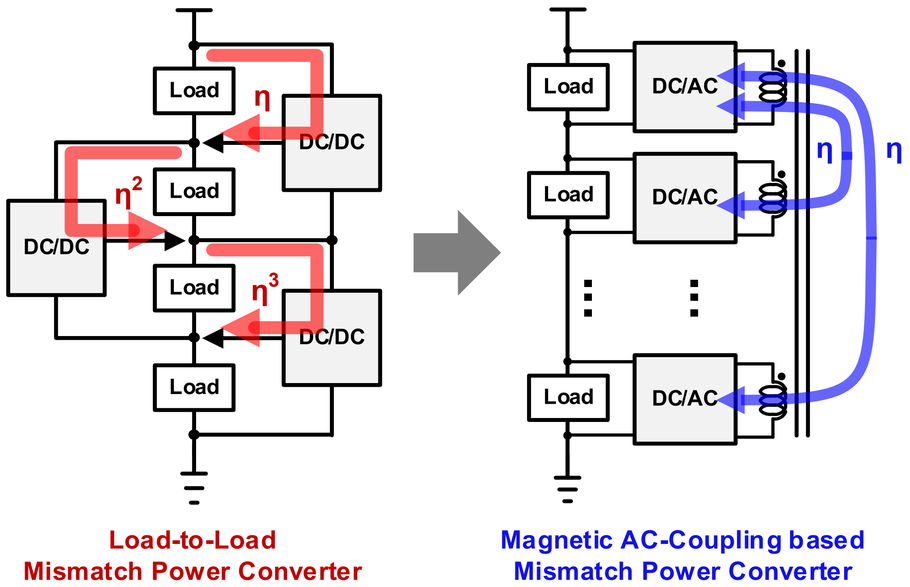
Voltage-Stacked Power Delivery

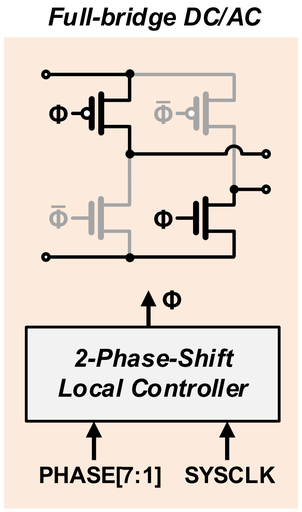
- Voltage stacking enables inherent high-voltage low-current power delivery.
  → Lower I^2R loss in power delivery network.
- Converter only drives mismatch power → High efficiency.



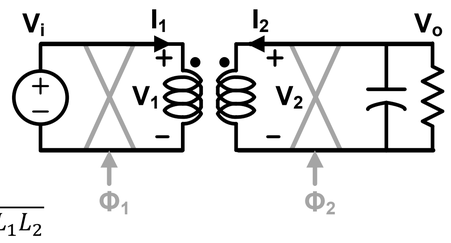
Magnetically AC-Coupled Mismatch Power Converter

- Load-to-Load: efficiency drops as current passes through multiple DC/DC.
- Magnetically AC-Coupled: every load is coupled through one transformer
  → Higher efficiency can be achieved.
- 2-Phase-Shift Controller is proposed for higher power density.





Power Transfer Mechanism



$M = k\sqrt{L_1 L_2}$

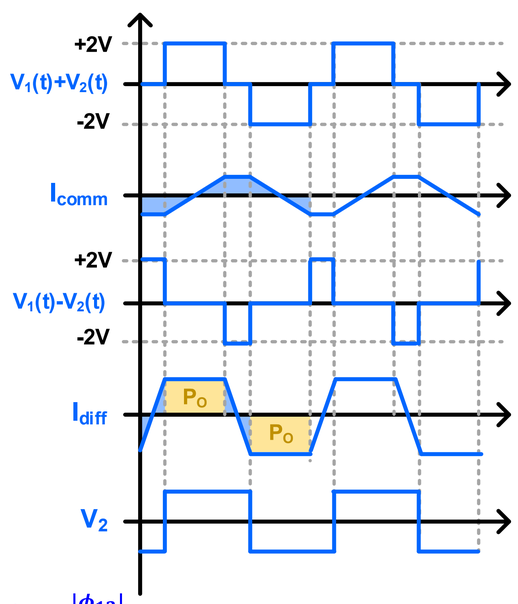
- $V_1(t) = L\frac{dI_1(t)}{dt} + M\frac{dI_2(t)}{dt}$ $\quad \overset{let}{I_1} = I_{comm} + I_{diff}$
- $V_2(t) = L\frac{dI_2(t)}{dt} + M\frac{dI_1(t)}{dt}$ $\quad I_2 = I_{comm} - I_{diff}$

- $I_{comm} = \frac{I_1+I_2}{2}$ $\quad$ • $I_{diff} = \frac{I_1-I_2}{2}$

➢ $\frac{dI_{comm}}{dt} = \frac{V_1(t)+V_2(t)}{2(L+M)}$ $\quad$ ➢ $\frac{dI_{diff}}{dt} = \frac{V_1(t)-V_2(t)}{2(L-M)}$

- $\Delta I_{diff} = \int_0^{\frac{\phi_{12}}{2\pi}T_s} \frac{2V}{2(L-M)}dt = \frac{V\cdot\phi_{12}\cdot T_s}{2\pi(L-M)}$
- $P_o = V \times \Delta I_{diff} \times \left(1 - \frac{|\phi_{12}|}{\pi}\right) = \frac{V^2}{2\pi f_s(L-M)}\phi_{12}\left(1 - \frac{|\phi_{12}|}{\pi}\right)$
- Maximum power flow when $\phi_{12} = \pi/2$

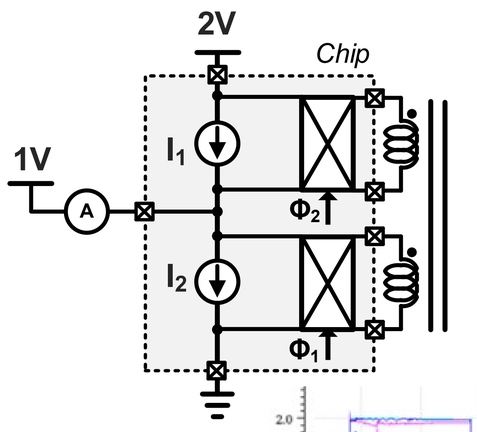
$0 < \phi_{12} < \pi/2$



Proposed 2-Phase-Shift Controller

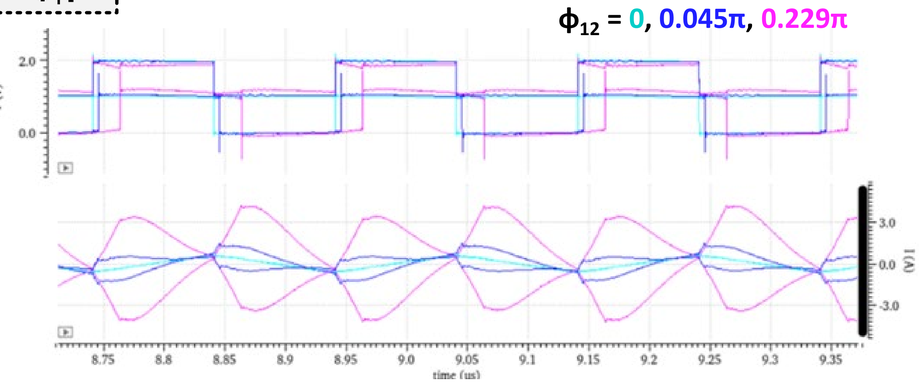
- Phase shift is updated by half in two steps.
  → DC current can be inherently cancelled without huge blocking capacitors.

Simulation results

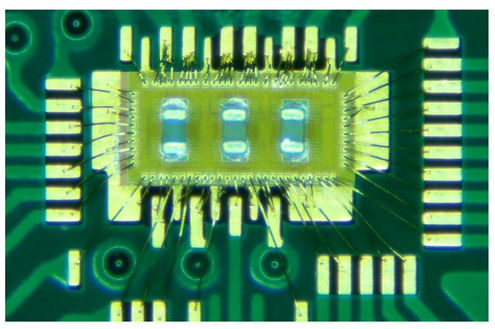


ϕ_{12}	$I_{DC,CONV}$ [A]	Efficiency (%)
0	0	-
0.045π	0.378	91.3
0.229π	1.95	82.5

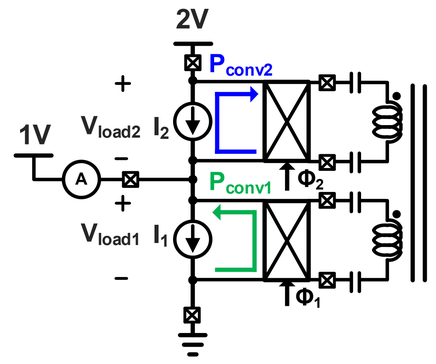
ϕ_{12} = 0, 0.045π, 0.229π



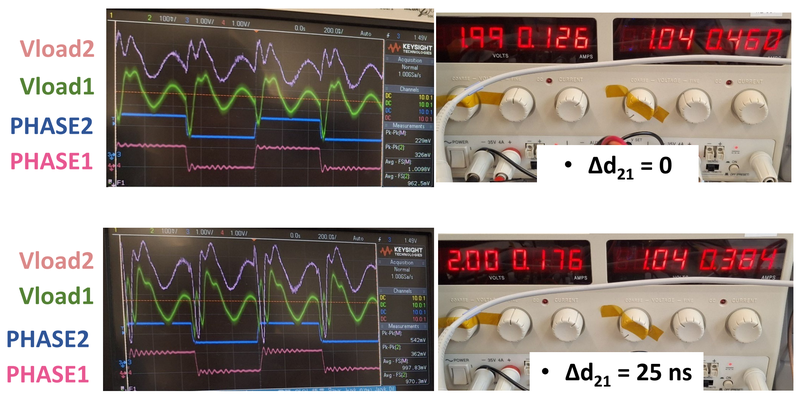
Chip Photo, Measurement Results



Chip Photo for 3-Stack
Magnetically AC-Coupled Converter



Measurement setup for 2-Stack Verification



$I_{load2} - I_{load1} = 0.62$ A *(idle)*

- P_{conv2} = 48 mW
- P_{conv1} = 27 mW
- η_{conv} = 56%

- Insufficient input decoupling
  → supply ripple
- High on-chip ESR
  → used higher-L XFMR
  → lower output power & efficiency

Acknowledgement and Reference

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

[1] Wang, Ping, et al. "Differential power processing for ultra-efficient data storage." IEEE Transactions on Power Electronics 36.4 (2020): 4269-4286.

[2] Candan, Enver, Pradeep S. Shenoy, and Robert CN Pilawa-Podgurski. "A series-stacked power delivery architecture with isolated differential power conversion for data centers." IEEE Transactions on Power Electronics 31.5 (2015): 3690-3703.

[3] Chen, Yenan, et al. "Power flow control in multi-active-bridge converters: Theories and applications." 2019 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, 2019.

[4] Qi, Yang, et al. "Decentralized Control for a Multi-active Bridge Converter." IEEE Transactions on Industrial Electronics (2022).

[5] Chattopadhyay, Ritwik, et al. "Sensorless phase shift control for phase shifted DC-DC converters for eliminating DC transients from transformer winding currents." 2018 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, 2018.