IDEC Chip Design Contest

A 6-bit 8GS/s Time-Interleaved Pseudo-Loop-Unrolled SAR ADC

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Introduction

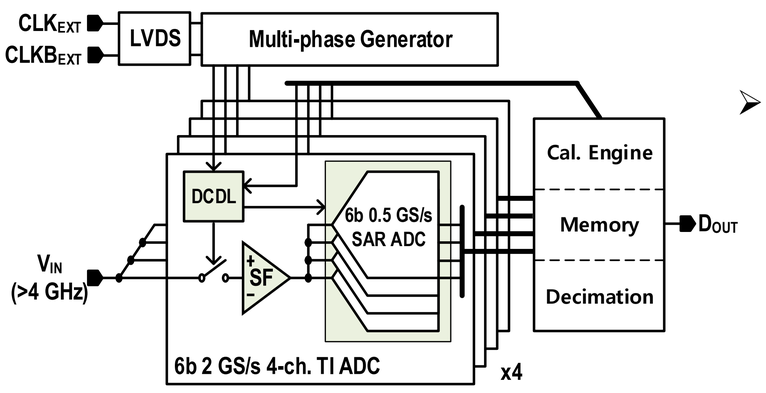
➢ **Asynchronous Pseudo Loop-Unrolled TI-SAR ADC (16-channel)**
- ✓ 16× time-interleaved architecture → Significant sampling rate enhancement
- ✓ Using one CDA per sub-ADC → Reduce offset calibration burden
- ✓ Loop-unrolled conversion → Eliminate register delay
- ✓ BD-ST-CDA's async. clock → Eliminate external high-speed global clock

➔**Achieves faster conversion than conventional SAR ADCs**

➢ **Complementary Dynamic Amplifier (CDA)**
- ✓ Current reuse → Improve power efficiency
- ✓ Twice conversion during one CLK period
- ✓ Reduce CLK driver & power consumption
- ✓ Generate asynchronous clock without metastability

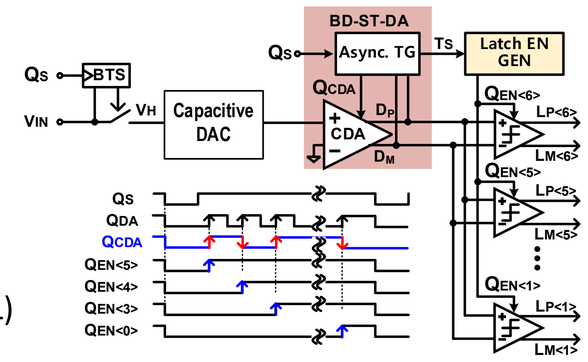
➔**Suitable for multi-channel TI structure with reduced clock distribution overhead**

Proposed 16-channel PLU TI-SAR ADC



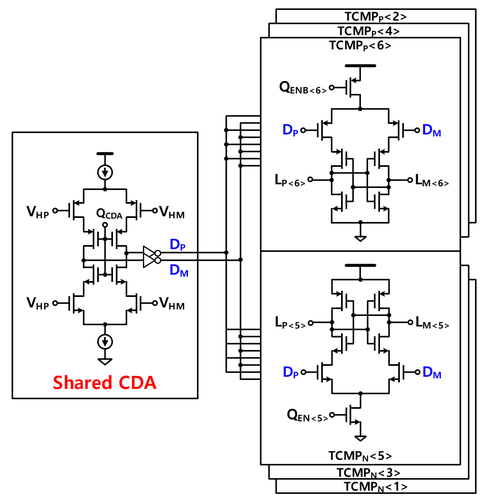
[16-ch TI PLU SAR ADC block diagram]

➢ **16-Channels Time-Interleaved SAR ADC**
- ✓ 6-bit 8-GS/s Analog-to-Digital conversion
- ✓ Channel mismatches
  - Offset: on-chip foreground calibration
  - Gain: no need
  - Time skew: on-chip digital calibration (DCDL)

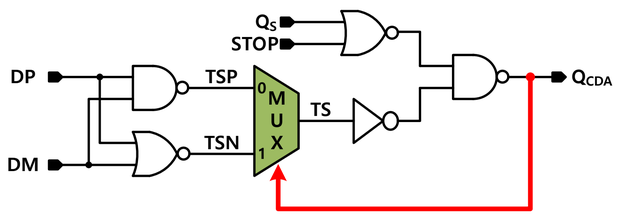


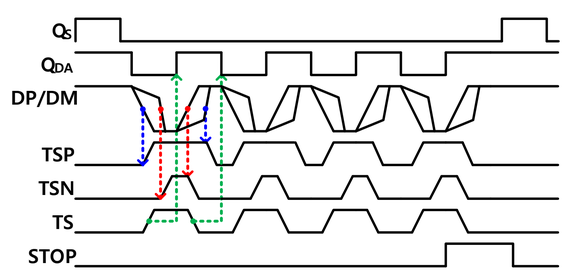
[Block diagram of the proposed PLU SAR ADC]

➢ **Proposed CDA and TCOMP**
- ✓ CDA-based voltage-to-time conversion
- → Sampled input → amplified to timing information
- ✓ Register-free loop-unrolled operation
- → TCMP output directly drives the capacitive DAC
- ✓ Bidirectional self-triggered QCDA
- → Enables asynchronous conversion sequence



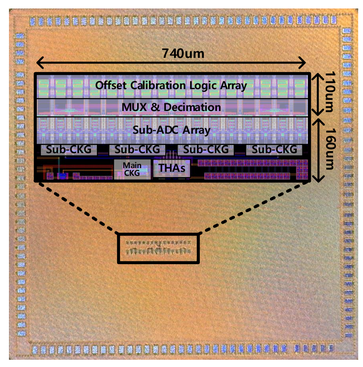
[Circuit diagram of a single CDA and subsequent six TCMPs.]





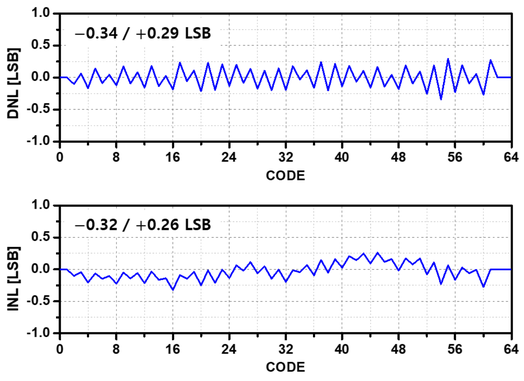
[Block and timing diagram of the proposed asynchronous timing generation logics]

➢ **Proposed CDA-based PLU SAR ADC**
- ✓ CDA-based PLU SAR ADC
- → Reduce offset-mismatch burden
- ✓ One asynchronous CDA + six TCMPs
- → Achieve 6-bit loop-unrolled conversion
- ✓ Halved async clock frequency by BD-ST-DA
- → Reduce clock-driving current and improve power efficiency

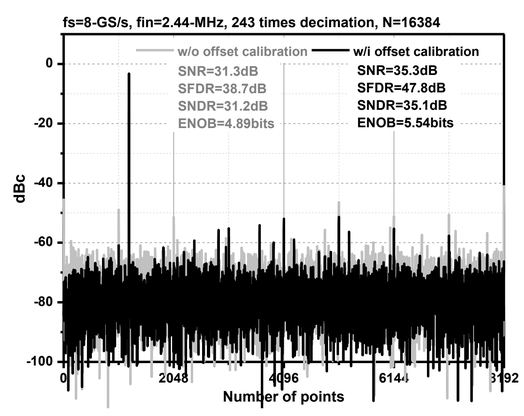


[Chip photograph]

➢ **Complementary Dynamic Amplifier (CDA)**
- ✓ Polarity-based selection (PMOS/NMOS)
- → Select appropriate timing signal according to CDA operation phase
- ✓ First-transition-based triggering
- → Minimize unnecessary timing delay
- ✓ Balanced delay for bidirectional operation
- → Improve overall SAR conversion speed



[Measured DNL and INL]



[Measured FFT spectra at low input frequency]

Conclusion

✓ 16-ch TI SAR ADC with CDA-based PLU architecture
✓ Single-CDA and dual-edge operation improving bandwidth and power efficiency
✓ 6-bit 8-GS/s 35.1dB SNDR (5.53 ENOB) and 47.8dB SFDR

Acknowledgement

✓ The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

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