Timing-Skew Calibration Using Absolute-Value Operation Between Adjacent Channels for 4-channel SAR ADC

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Introduction

➢ **Time-Interleaved(TI) ADC Architecture**
- ✓ Parallel operation of multiple ADC channels
- ✓ Increase the overall sampling speed
- ✓ Channel mismatches → degrades ADC performance

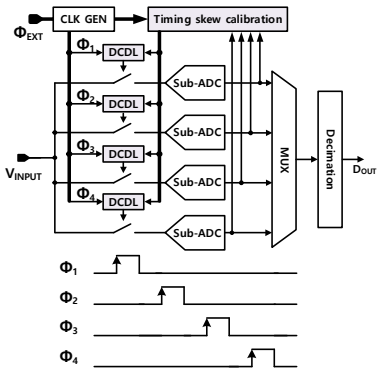
➔ **Mismatch calibration is necessary**

➢ **Proposed Calibration Algorithm**
- ✓ Absolute-based method → eliminate multipliers

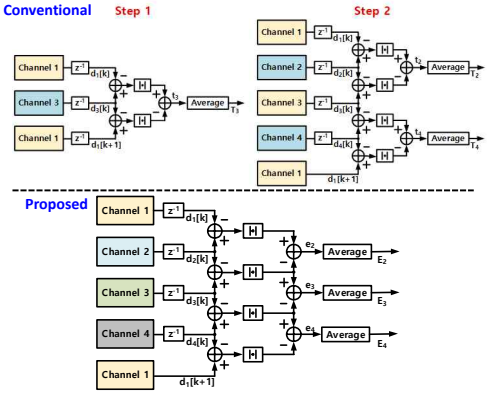
➔ **Reduce hardware overhead & area**
- ✓ Iterative calibration between adjacent channels

➔ **Enable Calibration up to the Nyquist frequency**

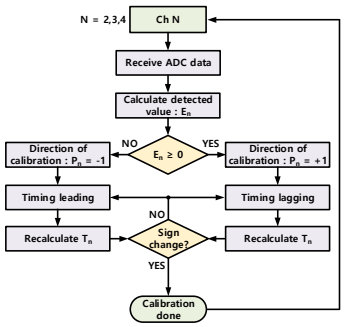
Proposed Calibration Algorithm and 4-channel SAR ADC



[4-ch TI SAR ADC block & timing diagram]



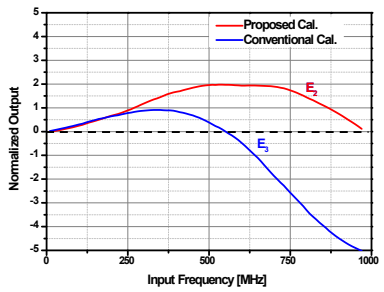
[Block diagram of the calibration technique]



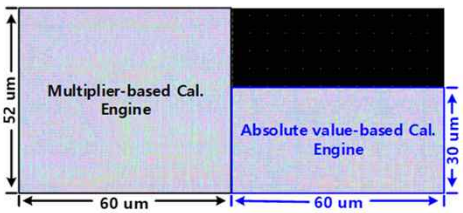
[Algorithm of the proposed timing skew cal]

➢ **4-ch TI ADC with Timing skew calibration**
- ✓ DCDL-based calibration minimizes inter-channel timing skew in the 4-ch TI SAR ADC.

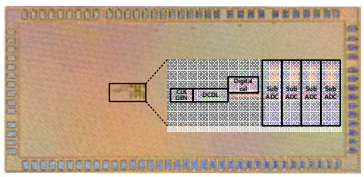
➢ **Proposed Calibration Method**
- ✓ Absolute-value operation removes the multiplier, reducing circuit area
- ✓ Adjacent-channel iterative calibration enables timing-error detection up to the Nyquist frequency



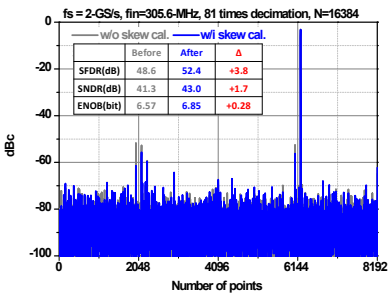
[Skew Error Detection vs. Input Frequency]



[Area reduction by multiplier removal]



[Chip photograph]



[Measured FFT spectra at 2-GS/s]

➢ **Observed Issues in the Proposed Calibration Design**
- ✓ Calibration operates correctly up to a 300-MHz input frequency at a 2-GS/s sampling rate
- ✓ Timing-skew calibration fails at higher input frequencies
- ✓ In addition, the calibration range is insufficient regardless of the input frequency
- ✓ These issues are presumed to be caused by the absolute-value circuit design and insufficient error-calculation samples

➔ **Future work will redesign the absolute-value circuit, optimize the DCDL full range and step size, and increase the number of samples for error calculation**

Conclusion

- ✓ 4-ch TI SAR ADC with timing-skew calibration
- ✓ Multiplier-free calibration using absolute-value operation
- ✓ Nyquist-rate timing-error detection with adjacent-channel iterative calibration
- ✓ 8-bit 2-GS/s 43dB SNDR (6.85 ENOB) and 52.4dB SFDR

Acknowledgement

✓ The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.