A 4-channel 8-bit 3.2-GS/s Time interleaving SAR-Flash ADC

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Introduction

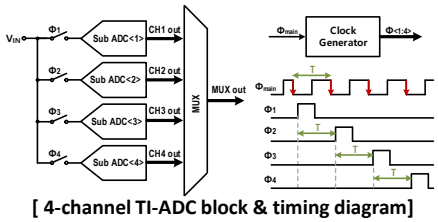
➢ **Asynchronous Loop-Unrolled SAR – IP Flash TI-SAR ADC (4-channel)**
- ✓ 4× time-interleaved architecture → Significant sampling rate enhancement
- ✓ Loop-unrolled conversion → Eliminate register delay
- ✓ SAR – flash 2step→ Improves resolution and sampling speed

➔**Achieves faster conversion than conventional SAR ADCs**

➢ **Complementary Dynamic Amplifier (CDA)**
- ✓ Current reuse → Improve power efficiency
- ✓ Twice conversion during one CLK period
- ✓ Reduce CLK driver & power consumption
- ✓ Generate asynchronous clock without metastability

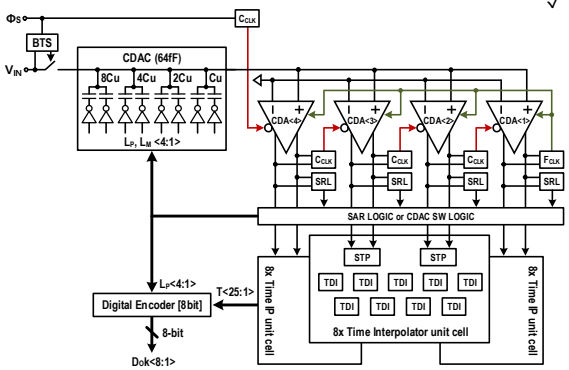
➔**Suitable for multi-channel TI structure with reduced clock distribution overhead**

Proposed 4-channel SAR-Flash ADC

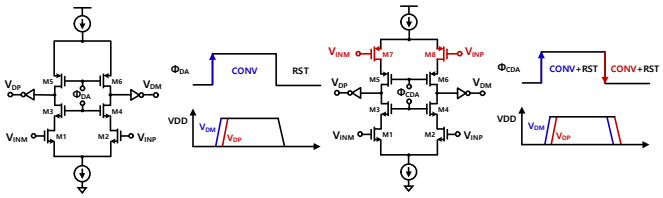


[4-channel TI-ADC block & timing diagram]

➢ **4-Channels Time-Interleaved ADC**
- ✓ 8-bit 3.2-GS/s Analog-to-Digital conversion
- ✓ Offset : on-chip foreground calibration (Gain: no need)
- ✓ Timing skew : on-chip Voltage-Controlled Delay Line(VCDL)-based phase-alignment scheme
  - → 4-channels include VCDL and 8-bit sub-ADC
  - → adjusts each sampling phase with fine resolution
- ✓ The measured SNDR appears to be limited by inter-channel gain mismatch.

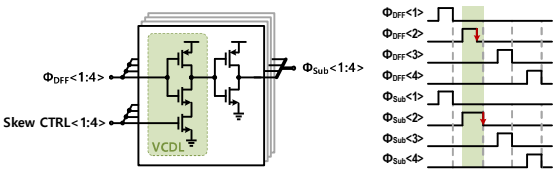


[Sub-ADC architecture]

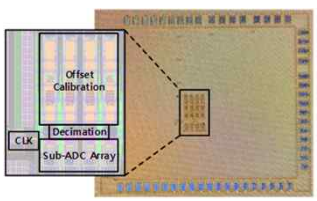


[DA&CDA circuit and timing diagram]

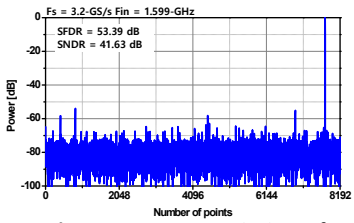
➢ **Complementary Dynamic Amplifier (CDA)**
- ✓ Polarity-based selection (PMOS/NMOS)
  - → Select appropriate timing signal according to CDA operation phase
- ✓ PMOS-assisted MSB decision and NMOS-assisted LSB decision
  - → Use PMOS operation for coarse MSB decision and NMOS operation for fine LSB decision
- ✓ First-transition-based triggering
  - → Minimize unnecessary timing delay
- ✓ Balanced delay for bidirectional operation
  - → Improve overall SAR conversion speed



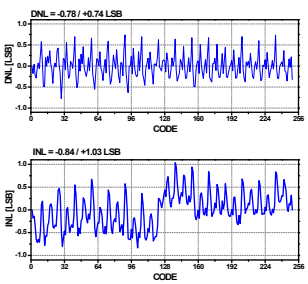
[VCDL circuit and timing diagram]



[Chip photograph]



[Measured FFT spectra at Nyquist input frequency]



[Measured DNL and INL]

Conclusion

✓ 4-channel 8-bit 3.2-GS/s TI SAR–Flash ADC
✓ VCDL-based timing-skew calibration with sampling-phase adjustment
✓ CDA-based asynchronous conversion with reduced clock distribution overhead
✓ Achieved 41.63-dB SNDR and 53.39-dB SFDR

Acknowledgement

✓ The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.