IDEC Chip Design Contest

A Low-Power MRAM-Based Non-Volatile Flip-Flop Architecture for Register and System-Level Applications

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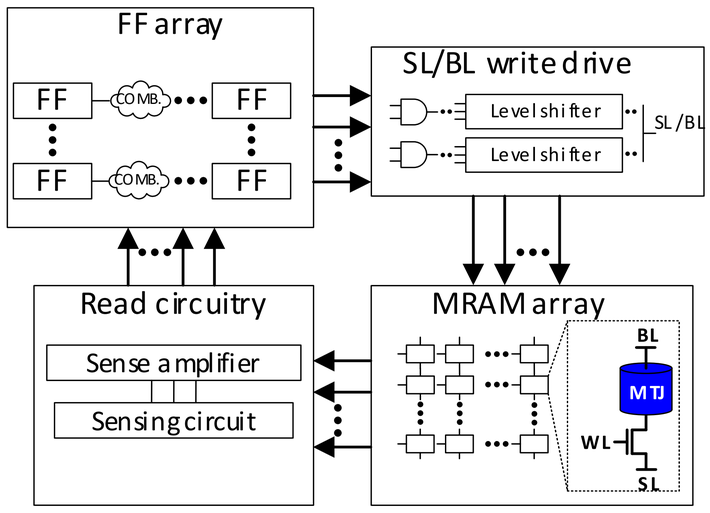
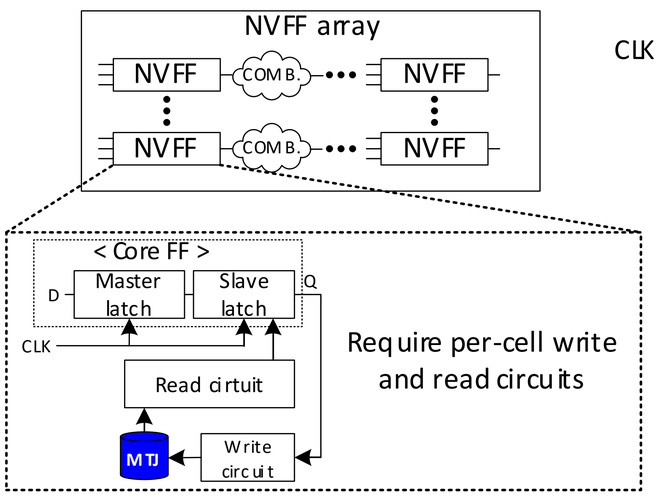
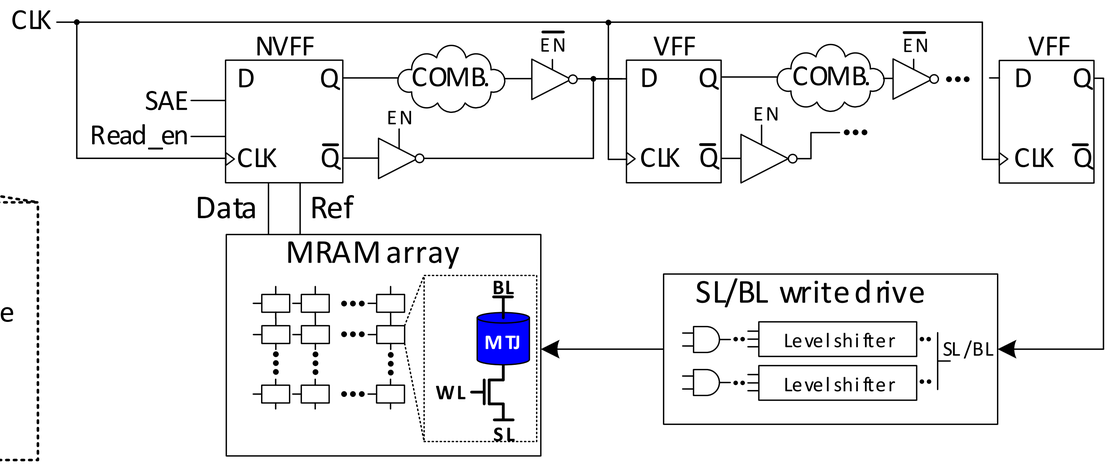
Introduction



eMRAM NVFF



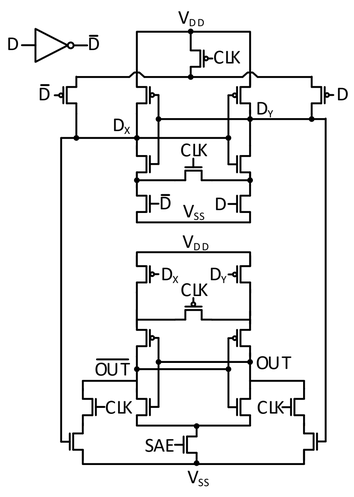
In-situ NVFF



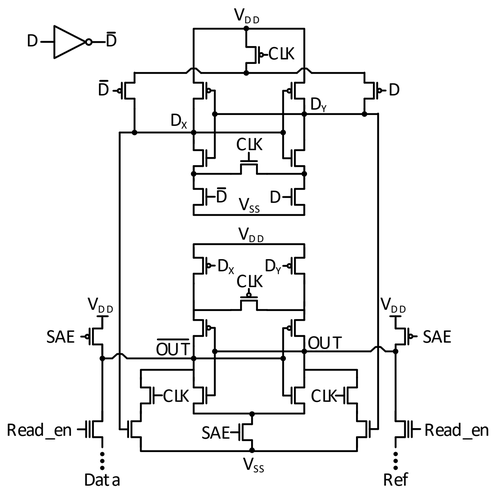
Proposed minimal-NVFF hybrid architecture

Over the years, two NVFF architectures have been explored: dual-macro designs, known as eMRAM NVFF, which require data transfer during store operations and incur area and latency overhead, and in-situ NVFFs that integrate nonvolatile devices within flip-flops to reduce data movement. Despite MRAM commercialization since 2012 and extensive research over the past decade, in-situ NVFFs remain largely prototypical due to the need for per-cell write drivers, control logic, and sensing circuits, resulting in significant area and power overhead. To address this limitation, we propose a minimal-overhead hybrid NVFF architecture that combines the simplicity of dual-macro schemes with the data-locality advantages of in-situ designs by employing a single NVFF for backup/restore and low-power SCDFF-based VFFs for the remaining array, thereby reducing peripheral overhead while enabling reliable near-threshold operation..

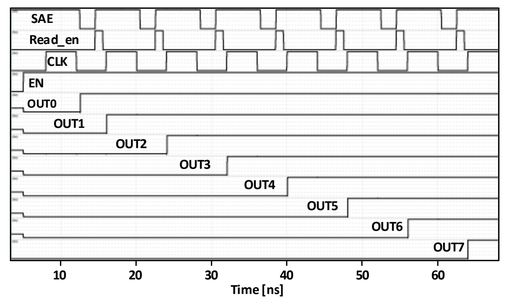
SCDFF and proposed nvSCDFF designs



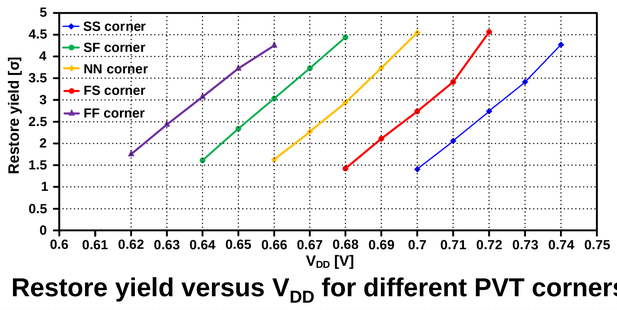
SCDFF



Proposed nvSCDFF



The restore operation of the proposed NVFF architecture (1 NVFF + 7 VFF) for an 8-bit configuration.

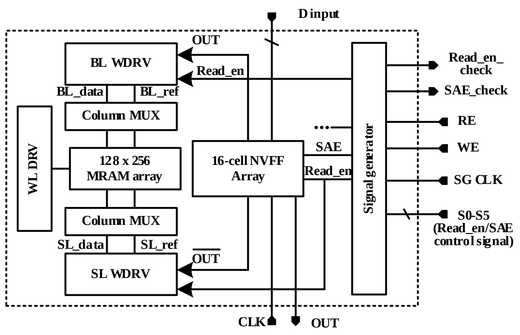


Restore yield versus V_{DD} for different PVT corners.

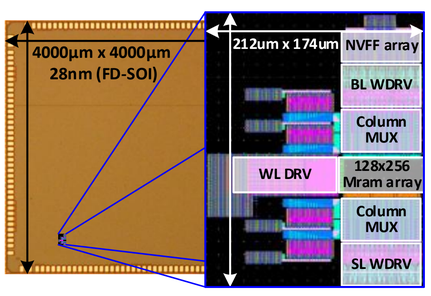
Because MTJ switching is stochastic, achieving low write-error rates at short latency requires high write current, leading to large per-cell write drivers and poor scalability in conventional in-situ NVFFs. To address this, the proposed architecture employs a single nvSCDFF located at the head of the array, while all remaining cells are implemented using compact SCDFF-based VFFs, thereby eliminating per-cell driver and sensing overhead.

Unlike prior NVFFs that rely on TGFFs, which incur high clock power and degrade at low V_{DD}, the proposed design adopts a static contention-free differential flip-flop (SCDFF) for improved robustness and energy efficiency. By minimally extending the SCDFF into an nvSCDFF, the design enables self-referenced sensing through differential MTJ discharge, achieving full-swing output restoration without a dedicated sense amplifier while preserving a symmetric and compact structure.

Simulation and test-chip measurment results



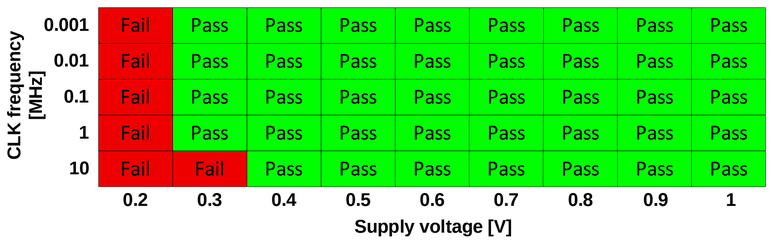
Test chip structure



Chip photo and layout view

Chip summary

	Normal Mode	Restore Mode
CMOS Technology	28nm FD-SOI	
Chip Area	36888µm²	
NVSCDFF Area	72 µm²	
Clock Frequency	10MHz	1MHz
Supply voltage	0.4V	0.65V



Test-chip shmoo plot of V_{DD} versus clock frequency indicating pass/fail regions of nvSCDFF operation

Metrics	Conventional in-situ NVFF architecture	Proposed minimal-NVFF hybrid architecture
Layout Size [µm²]	2848	1162
Normal mode energy @α =15% [pJ]	1.899	
Restore energy [pJ]	0.156	

Comparison of in-situ NVFF and proposed NVFF architectures for an 8-bit event counter.

Metrics	B. Song, TCAS-I 19' [10]	T. Na, ISCAS 14' [2]	M. Kazemi, TCAS-II 15' [14]	Proposed nvSCDFF
No. of transistors	50 + 2 Cap	47	24	28
Worst corner	SS	SS	SS	SS
Layout area (16-cell NVFF array) [µm²]	2840	2224	2496	1252
Average CQ delay [ps]	52.8[2]			50[1] / 57.3[2]
Power consumption @α =15% [nW]	1262.7			237.4
Restore yield @0.74V [σ]	>4[3]	>4[3]	>4[3]	>4[3] / 4.9[4]
Restore delay [ns]	4.5	0.9	0.604	0.607
Restore power [µW]	13.55	65.2	23.2	16.1
Restore energy [fJ]	61	56.68	14	9.7

1) For VFF
2) For NVFF
3) Simulation result.
4) Chip test result.

Comparison of proposed nvSCDFF with prior in-situ NVFF designs.

Conclusion

Simulation results using an 8-bit synchronous event counter show a 59% area reduction (2848 µm² → 1162 µm²) while maintaining comparable normal-mode and restore energy. At the cell level, the proposed nvSCDFF achieves ~2× area reduction (1,252 µm² vs. 2,224–2,840 µm²), 81% lower normal-mode power at 15% activity (237.4 nW vs. 1,262.7 nW), and 84% lower restore energy (9.7 fJ vs. 61 fJ) compared to TGFF-based NVFFs. Furthermore, chip measurements demonstrate robust restore reliability with a 4.9σ yield. These results highlight the proposed architecture as a scalable and energy-efficient solution for low-power, near-threshold, and instant-on applications such as IoT edge devices, always-on processors, and energy-constrained system-on-chip designs.