IDEC Chip Design Contest

Low Area Quadruple Node Upset-Tolerant and Self-Recoverable Latch Design with Recovery Signal for Aerospace Applications

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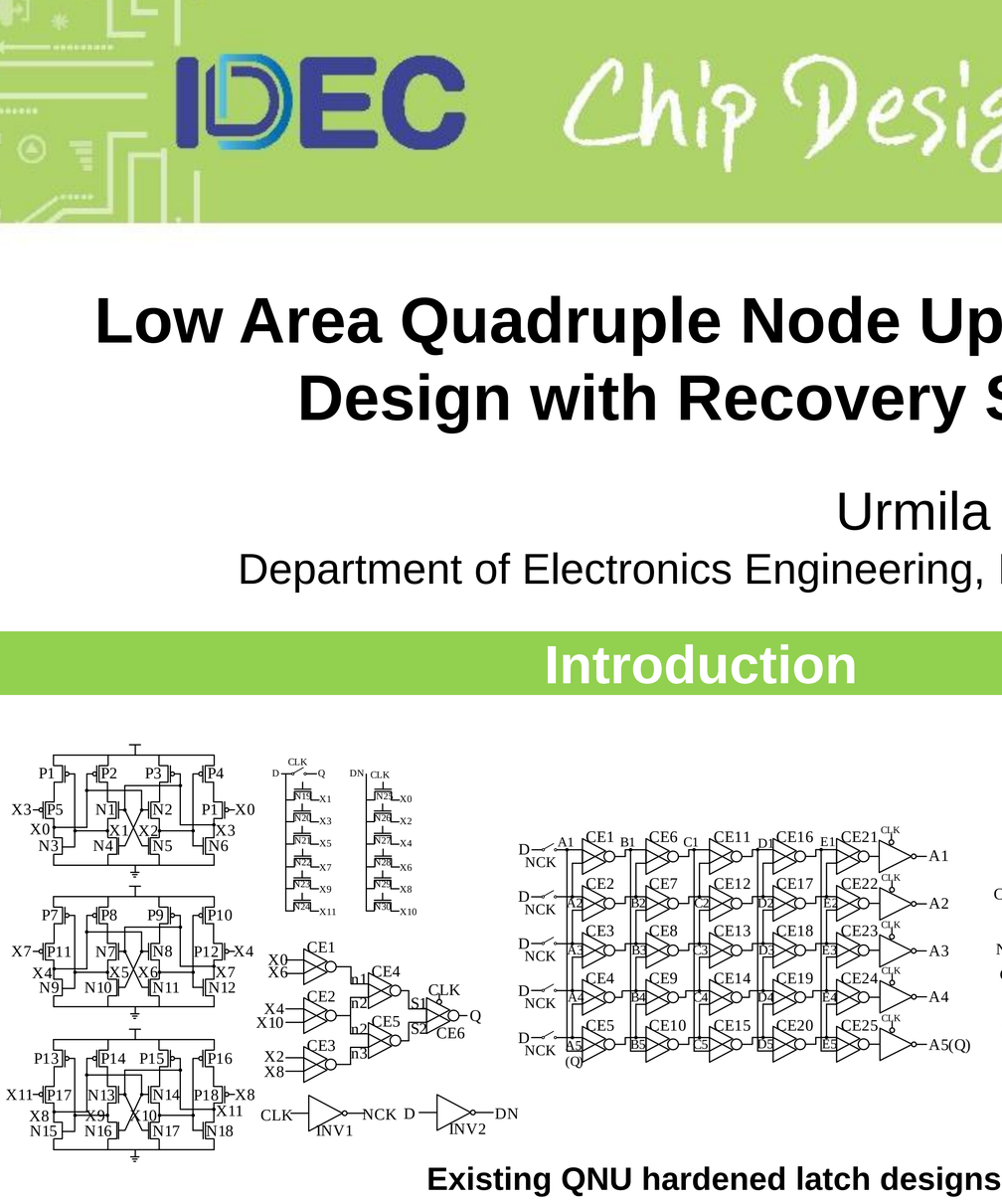
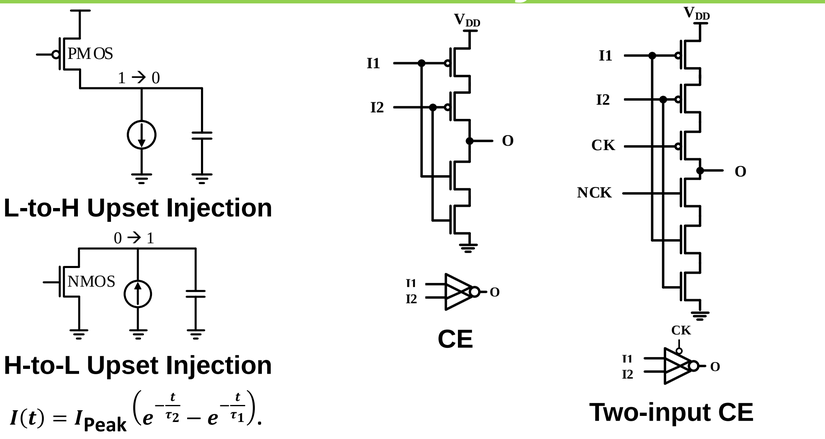
Introduction



Existing QNU hardened latch designs

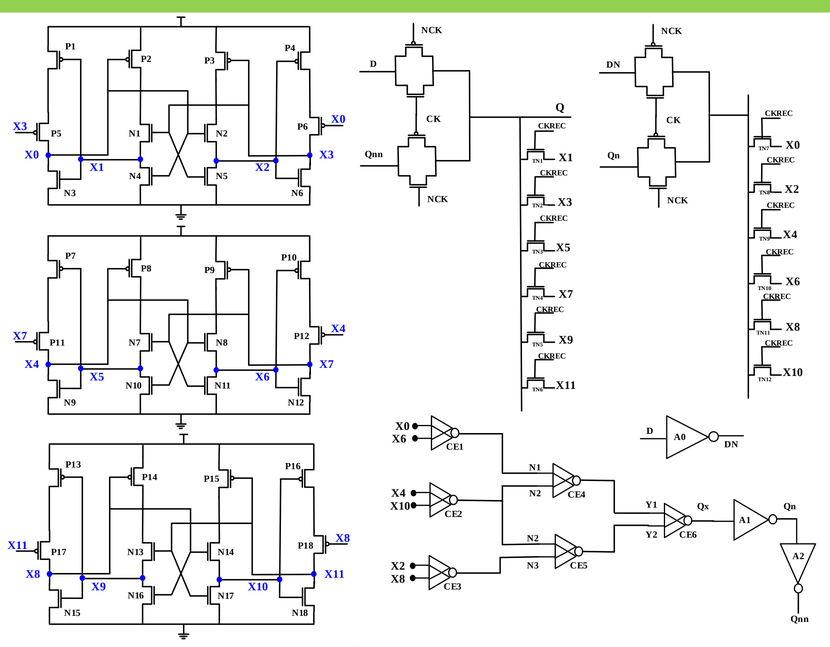
Advanced CMOS scaling has made circuits highly vulnerable to radiation-induced soft errors, particularly in aerospace environments. Single-event upsets (SEUs) and multiple-node upsets (MNUs) can corrupt data in latches, reducing system reliability. Existing hardened designs either incur large overhead or fail to ensure full recovery under severe conditions. This work proposes a low-area, fully self-recoverable QNU-tolerant latch (QNUTRL-RS) for robust and efficient operation.

Preliminary



Radiation-hardened latches rely on structures such as the C-element (CE), which preserves its state when inputs disagree, providing inherent soft-error resilience. While such designs improve tolerance to multi-node upsets, achieving full self-recovery under QNU remains challenging. Radiation effects are modeled using a double-exponential current source for low to high (L–H) and high to low (H–L) transitions, where I_{Peak} is the peak current, and τ_1, τ_2 are the rise and fall time constants.

Proposed circuit

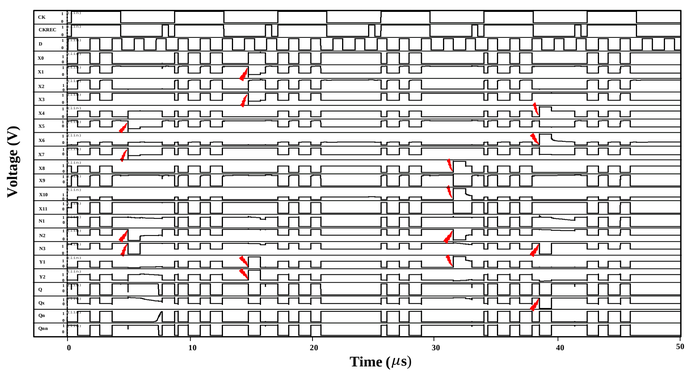


Proposed QNUTRL-RS latch design

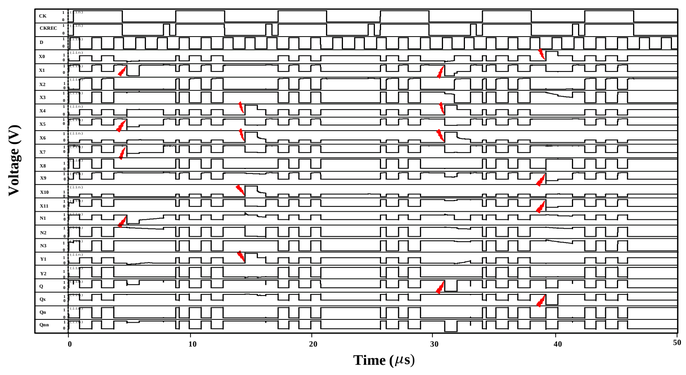
The proposed QNUTRL-RS latch enhances conventional SEI-based latch designs by integrating a CE tree and a recovery (REC) signal–controlled feedback mechanism. The latch employs three SEI SRAM cells for data storage, while the CE network stabilizes internal nodes by holding previous values when input disagreement occurs. In addition, two transmission switches controlled by CKREC enable both high-speed data propagation and controlled recovery paths.

QNUTRL-RS offers two key advantages over conventional QNU-tolerant latches:
First, it ensures complete self-recovery of disturbed nodes through the REC-assisted feedback mechanism. When node upsets occur, the correct logic values from Qn and Qnn are fed back to the affected nodes during hold mode, enabling full restoration even under severe QNU conditions.
Second, it improves stability and robustness by combining intrinsic CE-based recovery with external feedback. While the CE tree suppresses error propagation and stabilizes intermediate nodes, the REC signal reinforces recovery in cases where intrinsic mechanisms are insufficient, preventing error accumulation and floating states. Consequently, the proposed QNUTRL-RS latch achieves full self-recoverability from SNU, DNU, TNU, and QNU, while maintaining reduced delay, lower switching activity, and improved power–area efficiency compared to existing designs.

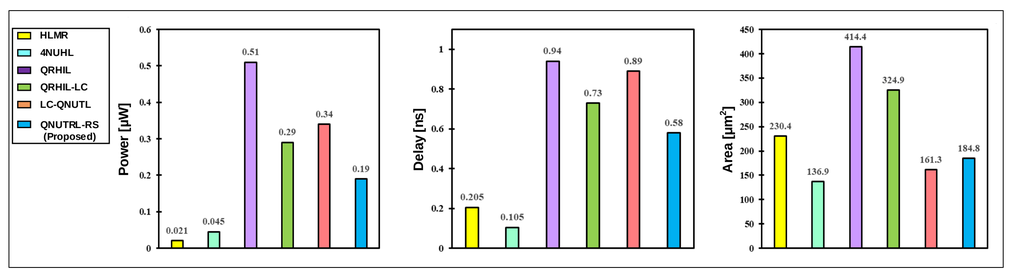
Simulation and test-chip measurment results



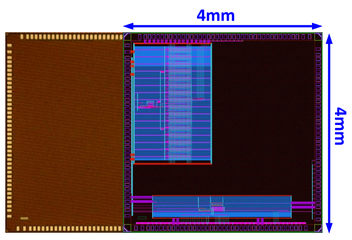
QNU cases affecting two nodes in an SEI SRAM cell and two nodes in the CE tree.



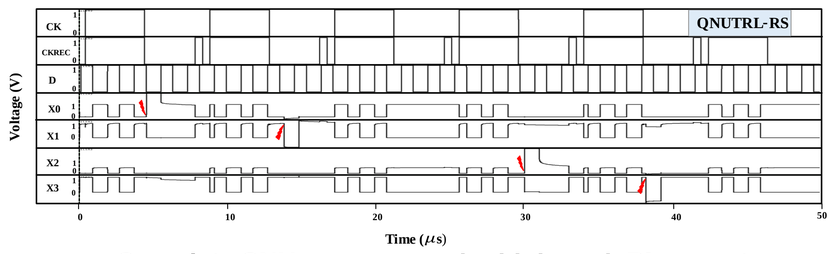
QNU cases across two nodes in one cell, one in another cell, and one in the CE tree.



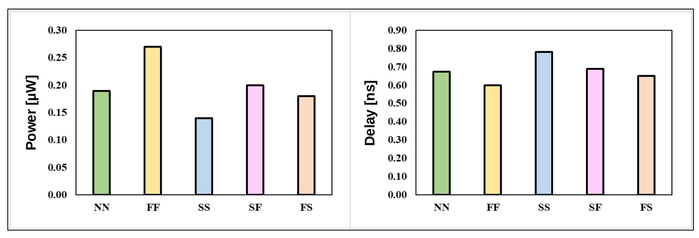
Comparison of latches in terms of average power, D–Q delay, and silicon area.



Chip photo and layout view



Complete SNU recovery under high peak RI current (500 µA, 1 µs)



Average power and D–Q delay across process corners

Latch	# of TRs	SNU Recoverable	DNU Recoverable	TNU Recoverable	QNU Tolerant	QNU Recoverable
HLMR [37]	96	√	√	√	-	-
4NUHL [38]	74	√	√	√	-	-
QRHIL [39]	130	√	√	√	√	√
QRHIL-LC [39]	114	√	√	√	√	√
LC-QNUTL [40]	80	√	-	-	-	-
Proposed QNUTRL-RS	86	√	√	√	√	√

Comparison of latches in terms of self-recovery capability and transistor count.

Conclusion

The proposed QNUTRL-RS latch achieves 100% self-recovery for SNU, DNU, TNU, and QNU, unlike conventional designs that either lack QNU recovery or only provide tolerance. With only 86 transistors, it maintains competitive area (184.8 µm²) while significantly improving efficiency, achieving 44.11% lower power and up to 38.43% lower delay compared to LC-QNUTL. Although some designs offer smaller area or lower delay, they fail to ensure full QNU recovery, limiting their reliability. These results demonstrate that the proposed latch provides an optimal balance of robustness, power, delay, and area, making it highly suitable for radiation-hardened aerospace applications. Preliminary chip measurements were unsuccessful due to non-functional silicon; however, post-layout simulation results consistently validate the effectiveness and robustness of the proposed design.