IDEC Chip Design Contest

Analysis of Low Area Digital Up/Down Clipping Counter for Digital In-Memory Computing

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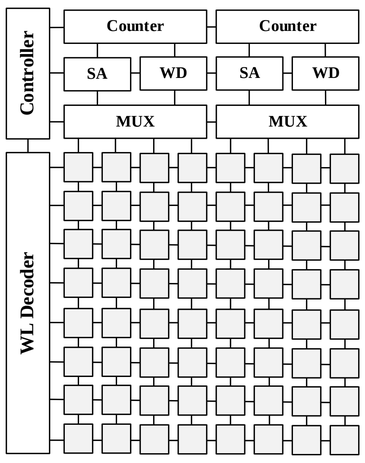
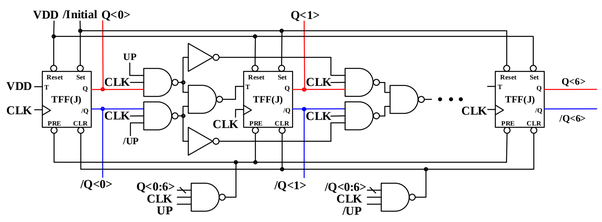
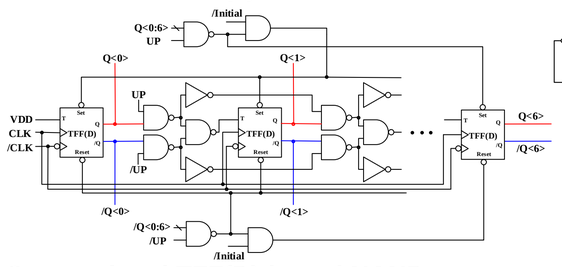
Introduction



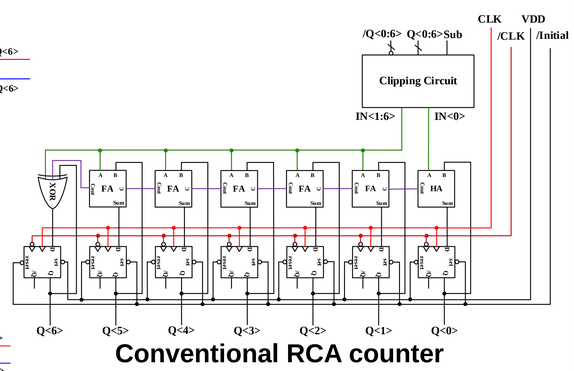
Ternary-output BNN



Conventional TFF(J)-based NAND counter



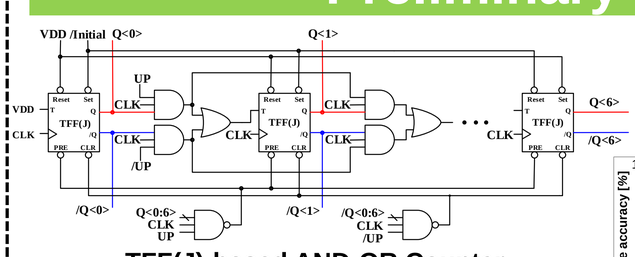
Conventional TFF(D)-based NAND counter



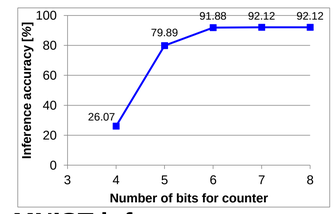
Conventional RCA counter

The ternary-output BNN employs a column-wise digital readout where accumulation is performed using counters, making their area and energy dominant factors in overall efficiency. To address this, we adopt a non-circular clipping counter to reduce bit-width and, through optimization and analysis, propose a novel RCA-based counter alongside a TFF-based implementation for efficient design trade-offs.

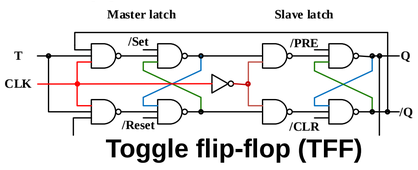
Preliminary



TFF(J)-based AND-OR Counter



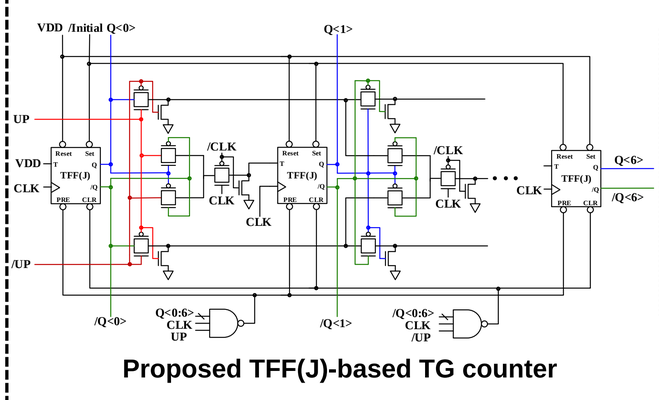
MNIST inference accuracy vs. counter bit-width for ternary-output BNN



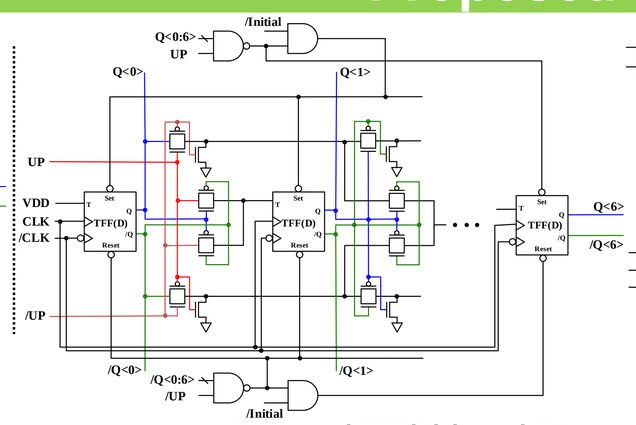
Toggle flip-flop (TFF)

Conventionally, the Up/Down Clipping Counter is a non-circular counter that performs bidirectional accumulation with saturation, preventing overflow and underflow; thus, since the PRE and CLR inputs of the JKFF are used for clipping, additional Set and Reset inputs are required to initialize the counter to 0111111. Accuracy analysis shows that a 7-bit counter achieves maximum inference accuracy, enabling bit-width reduction without performance loss.

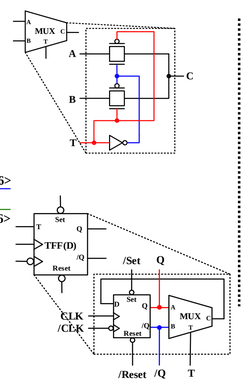
Proposed circuits

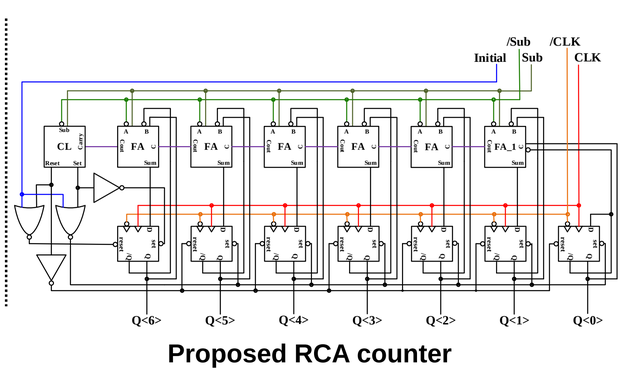


Proposed TFF(J)-based TG counter

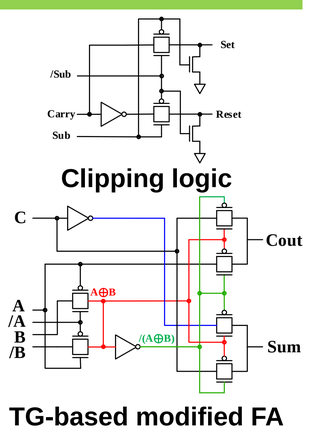


Proposed TFF(D)-based TG counter



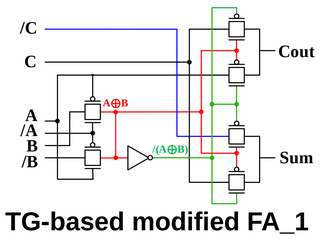


Proposed RCA counter



Clipping logic

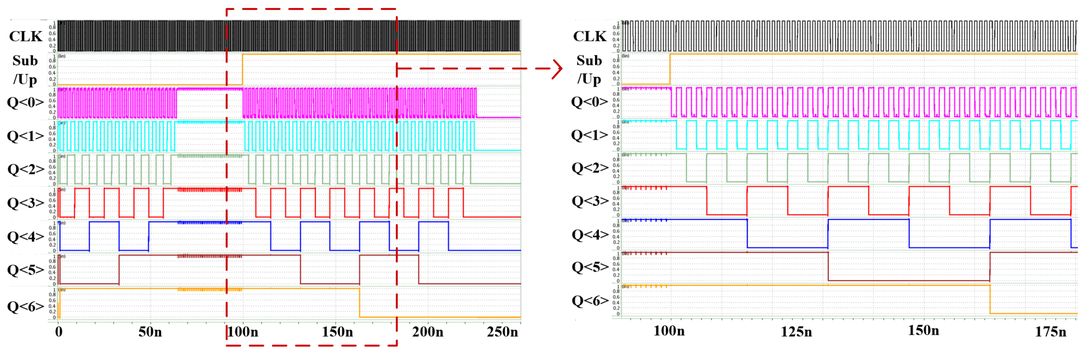
TG-based modified FA



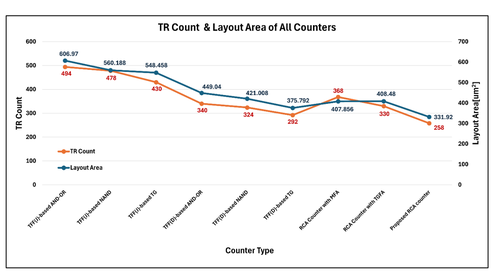
TG-based modified FA_1

Proposed TFF(J)-based TG Counter: Reduces area and power by replacing conventional NAND/AND–OR logic with transmission-gate (TG)-based logic, where the T determination function is efficiently implemented using a compact 2:1 MUX structure, significantly lowering transistor count.
Proposed TFF(D)-based TG Counter: Further reduces area and energy by replacing JKFF with DFF-based TFF, which requires fewer transistors and eliminates additional clock-related logic, thereby minimizing circuit complexity and overhead.
Proposed RCA Counter: Achieves the highest efficiency by eliminating conventional clipping circuits and utilizing carry-out-based clipping detection, while TG-based full adders, inverter removal, and simplified LSB logic further reduce transistor count and energy consumption.

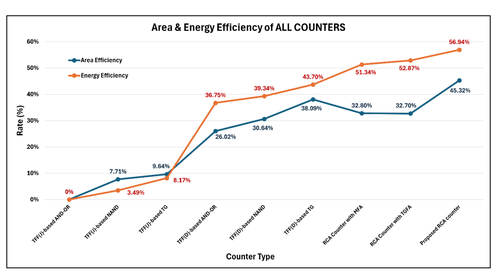
Simulation and test-chip measurment results



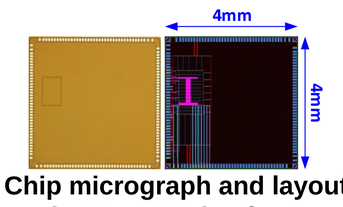
Transient response of the Proposed RCA Counter



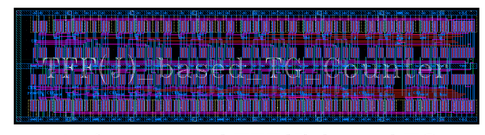
Transistor count and layout area comparison of all counters.



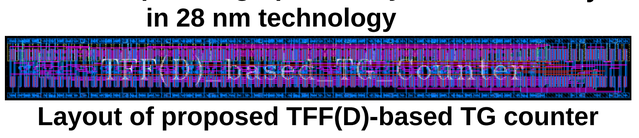
Area and energy efficiency of all counters



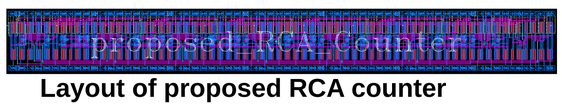
Chip micrograph and layout in 28 nm technology



Layout of proposed TFF(J)-based TG counter



Layout of proposed TFF(D)-based TG counter



Layout of proposed RCA counter

	TFF(J)-based Counter			TFF(D)-based Counter			RCA-based Counter		
Counter Type	AND-OR Counter	NAND Counter	**Proposed TG Counter**	AND-OR Counter	NAND Counter	**Proposed TG Counter**	RCA Counter with MFA	RCA Counter with TGFA	**Proposed RCA Counter**
Technology	**28 nm**								
Transistor Count	494	478	**430**	340	324	**292**	368	330	**258**
Layout Area	606.97 μm²	560.19 μm²	**548.46 μm²**	449.04 μm²	421.01 μm²	**375.79 μm²**	407.86 μm²	408.48 μm²	**331.92 μm²**
Area Efficiency	0 %	7.71 %	**9.64 %**	26.02 %	30.64 %	**38.09 %**	32.80 %	32.70 %	**45.32 %**
Average Power	269.40 μW	260.00 μW	**247.30 μW**	170.40 μW	163.40 μW	**151.60 μW**	131.10 μW	127.00 μW	**115.90 μW**
Average Energy	67.34 pJ	64.99 pJ	**61.84 pJ**	42.59 pJ	40.85 pJ	**37.91 pJ**	32.77 pJ	31.74 pJ	**28.98 pJ**
Energy Efficiency	0 %	3.49 %	**8.17 %**	36.75 %	39.34 %	**43.70 %**	51.34 %	52.87 %	**56.94 %**

Proposed RCA counter

Conclusion

The Proposed TFF(J)-based TG counter achieves 9.64% area and 8.17% energy reduction compared to the TFF(J)-based AND-OR counter, while a TFF(D)-based design improves this to 16.31% area and 10.99% energy reduction. The Proposed TFF(D)-based TG counter achieves up to 38.09% area and 43.70% energy reduction among TFF-based designs. RCA-based counters exhibit slightly larger area (~8.62%) despite reduced transistor count but offer superior energy efficiency, with up to 16.28% additional energy reduction over the Proposed TFF(D)-based TG counter. The Proposed RCA counter further improves both metrics, achieving 11.67% additional area reduction and 23.55% additional energy reduction, and up to 45.32% area and 56.94% energy reduction, demonstrating overall efficiency for low-power digital IMC applications.