IDEC Chip Design Contest

A Threshold-Logic Synaptic Memristor-Based Analog Neuromorphic PIM Array for Energy-Efficient Boolean Operation

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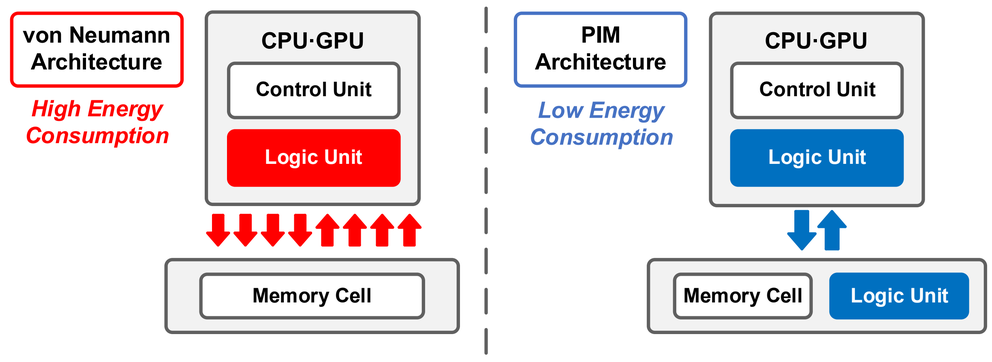
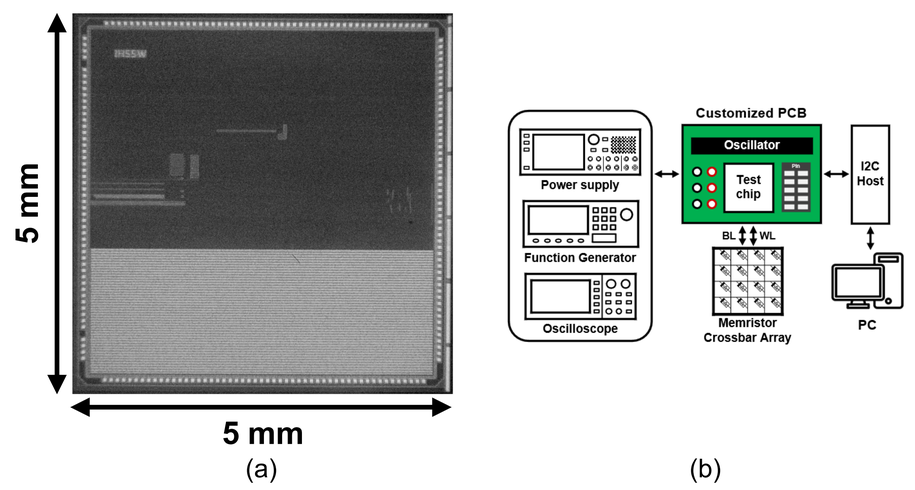
Introduction



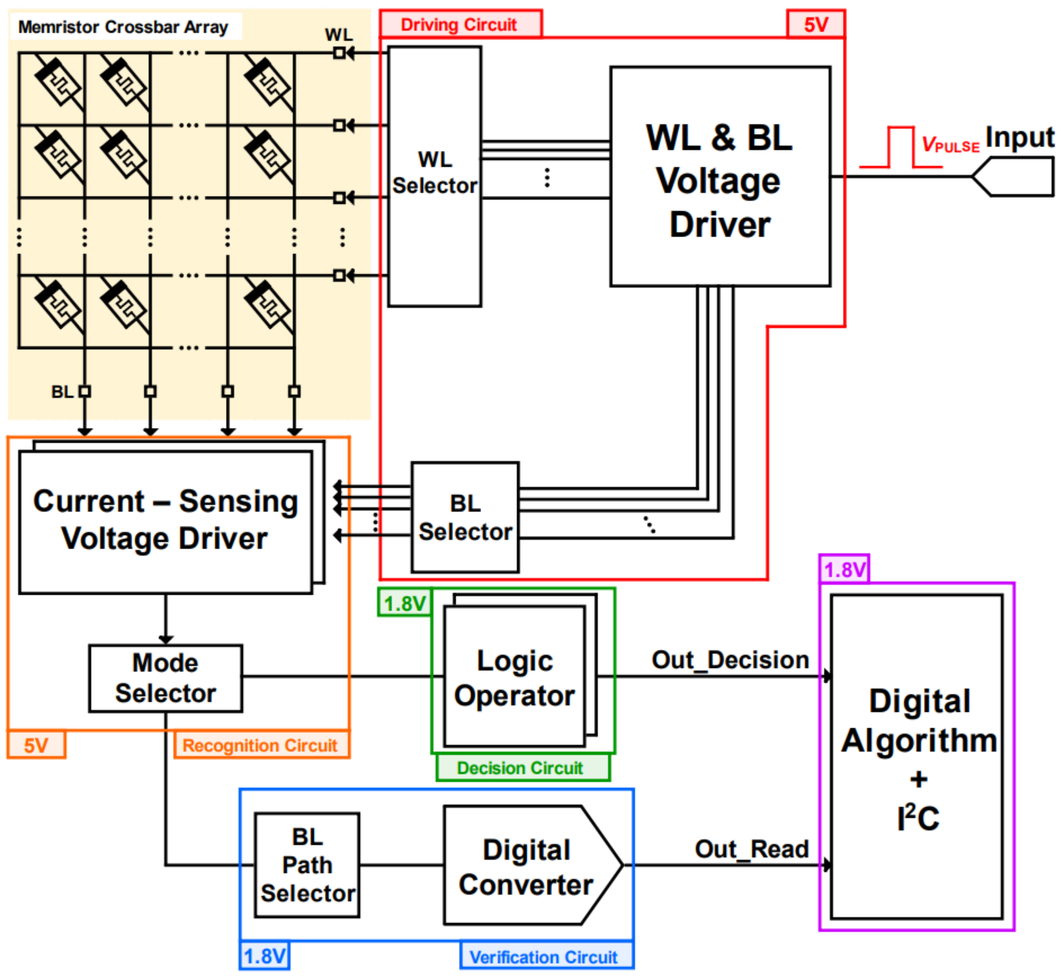
- With the rapid growth of AI, big data, and deep learning, the demand for energy-efficient, high-throughput data processing has intensified, positioning Processing-in-Memory (PIM) as a promising paradigm by enabling computation directly within memory.

Chip Micrograph & Measurement Setup



- (a) Chip Micrograph of the fabricated IC
- (b) Experimental setup for the proposed PIM IC

Proposed Memristor Crossbar Array Programming & Readout System Architecture



- The switch matrix selects the desired Word-Lines (WL) and Bit-Lines (BL) to configure the array for programming or read operations. It provides the required signal routing to access the target cells while preventing unwanted disturbance from unselected lines.
- The resulting bit-line currents are sensed by the current sensing voltage drivers (CSVD) and delivered to the decision array. The sensed current information is then used for reliable comparison and subsequent threshold logic evaluation.
- The programmed state of each cell is verified using a 7-bit SAR ADC. This verification step ensures that the programmed cell reaches the intended conductance level with sufficient accuracy.
- All control signals are managed by the full on-chip digital logic, which coordinates the overall operation of the system, including array selection, read/write timing, and verification sequencing.

Evaluation of Boolean Function and Reliability

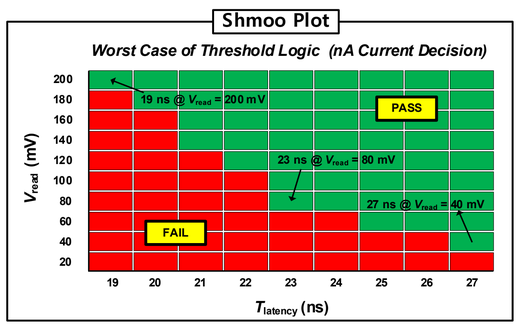
▪ 2-input Logic [Current unit : μA, Voltage unit : mV]

Boolean Function	MAX Current		MIN current		ΔI_{min}	ΔV_{min}
	Bit+	Bit−	Bit+	Bit-		
AB	7.5	6	0.5	5	1.5	155.7
A+B	10.5	3.75	0.5	2.75	2.25	101.87
(AB)'	6	7.5	5	0.5	1.5	155.7
(A+B)'	3.75	10.5	2.75	0.5	2.25	101.87

▪ 3-input, 4-input Logic [Current unit : μA, Voltage unit : mV]

Boolean Function	MAX Current		MIN current		ΔI_{min}	ΔV_{min}
	Bit+	Bit−	Bit+	Bit-		
ABC	7.25	6.5	0.5	5	1.5	155.7
A+B+C	15.5	4.25	0.5	2.75	2.25	56.28
AB+BC+CA	11	6.5	0.5	5	4.5	203.74
AB+AC	9.25	6.5	0.5	5	2.75	124.506
C+AB	11	5.5	0.5	4	3.5	158.46
(ABC)'	6.5	7.25	5	0.5	0.75	77.85
(A+B+C)'	4.25	15.5	2.75	0.5	2.25	56.28
ABCD	7.5	7	0.5	5	**0.5**	**51.9**
A+B+C+D	20.5	4.75	0.5	2.75	2.25	56.28
ABC+ABD+ACD+BCD	9.5	7	0.5	5	2.5	113.19
B+AC+AD+CD	13.75	6	0.5	4	3.5	158.46
C+ABD	11.5	6.5	0.5	4.5	3.5	158.46
(ABCD)'	7	7.5	5	0.5	**0.5**	**51.9**
(A+B+C+D)'	4.75	20.5	2.75	0.5	2.25	56.28

(a)



(b)

- (a) Current margin analysis for multi-input logic functions
- (b) Shmoo plot of readout voltage (V_{read}) vs. latency ($T_{latency}$)

Conclusion

- A memristor-based PIM IC was fabricated in 180-nm BCDMOS process with integrated programming, readout, and full on-chip digital control circuits.
- Sneak current suppression and 7-bit SAR ADC adoption minimized capacitive load and improved readout linearity and reliability.
- Measurement results validate successful multi-input Boolean operations, confirming feasibility for energy-efficient AI hardware applications.