IDEC Chip Design Contest

A 57-70 GHz 2-Stage 24dB Gain Control Range Variable Gain Amplifier with 0.5dB Resolution for Low-Phase-Error in 28nm CMOS Technology

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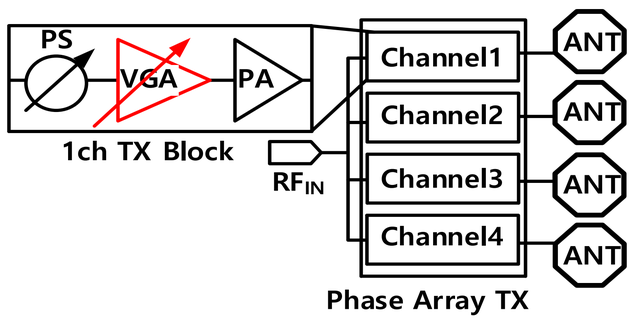
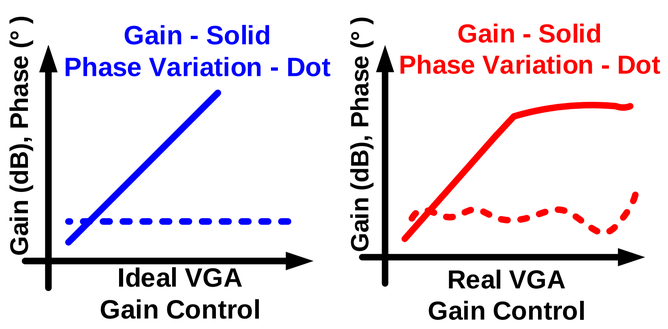
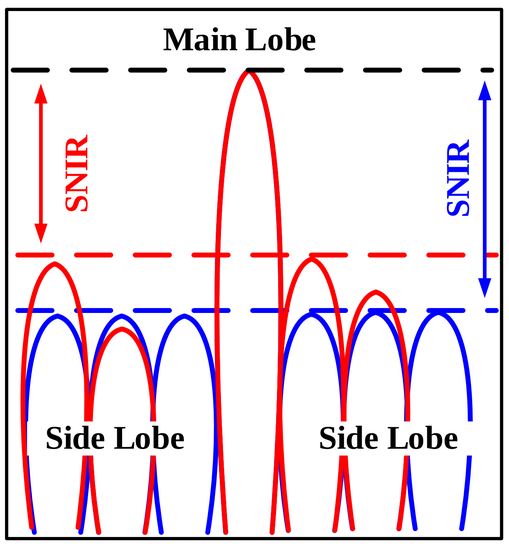
Introduction



Phase Array Transmitter



VGA Gain Control

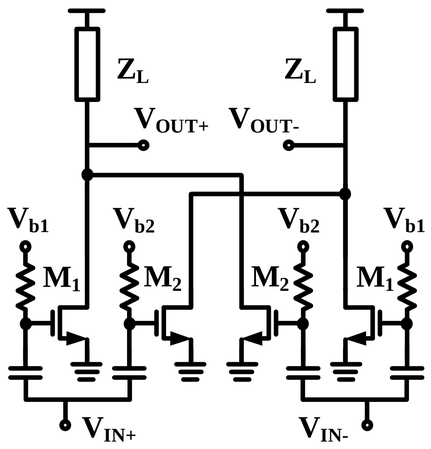


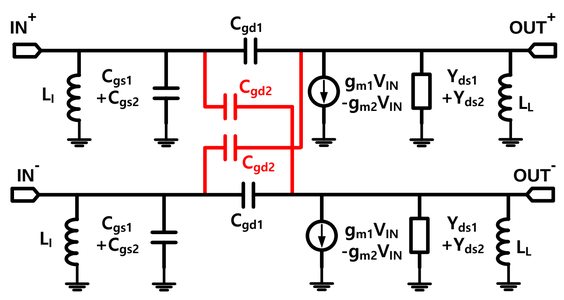
Beamforming Lobes

Phase Variation ➔ Side Lobe Increase

- High gain-range VGA induces phase variation
- AM-PM distortion of VGA is EVM deterioration
  ➔ High modulation limitation
- Phase variation increases side lobe
  ➔ SNIR degradation

Impedance Invariant VGA & Proposed 2-stage VGA





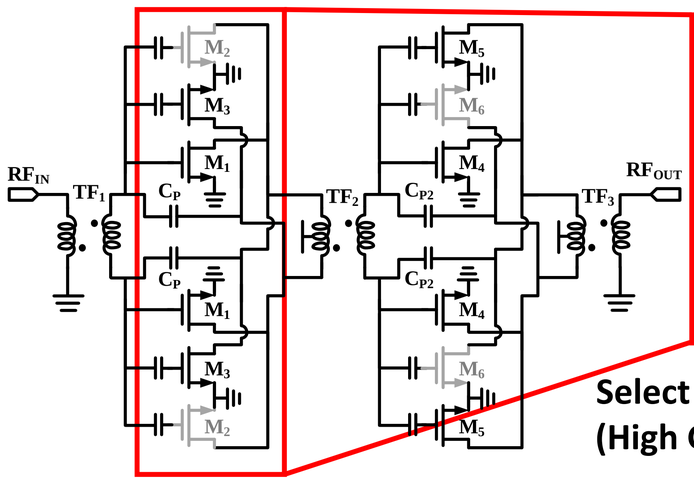
Voltage gain: $A_V = -\frac{(g_{m1}-g_{m2}-sC_{gd1}+sC_{gd2})}{sC_{gd1}+sC_{gd2}+Y_{ds1}+Y_{ds2}}$

Phase $\Delta\theta = tan^{-1}\left(\frac{-wC_{gd1}+wC_{gd2}}{g_{m1}-g_{m2}}\right)$

Impedance Invariant VGA Structure & Small Signal Model

If, Same TR Bias: $wC_{gd1} = wC_{gd2}$ ➔ $\Delta\theta = 0$ (Phase in variation)

But, TR Bias Variation: $wC_{gd1} \neq wC_{gd2}$ ➔ High Gain $\theta \neq$ Low Gain θ



Phase Variation at Gain Mode

High Gain Mode θ ($M_{1,2}$ On, M_3 Off)

$= tan^{-1}\left(\frac{-wC_{gd1}-wC_{gd2}+wC_{gd3}+wC_P}{g_{m1}+g_{m2}-g_{m3}}\right)$

Low Gain Mode θ (M_2 Off, $M_{1,3}$ On)

$= tan^{-1}\left(\frac{-wC_{gd1}-wC_{gd3}+wC_{gd2}+wC_P}{g_{m1}+g_{m2}-g_{m3}}\right)$

Select Optimized C_P for Low Phase Error
(High Gain Mode θ = Low Gain Mode θ)

8dB Gain Control Mode (M_2 Off, $M_{1,3}$ On)

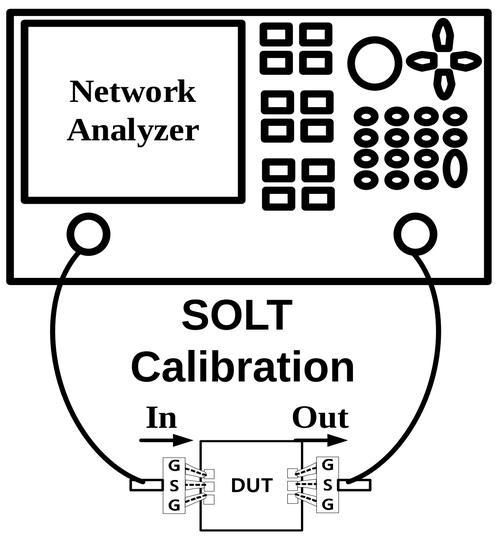
Transistor M_2 (M_5) = M_3 (M_6)
➔ $g_{m2} = g_{m3}$ / $C_{gd2} = C_{gd3}$

$C_P = C_{gd1,on} + \frac{g_{m1\,on}}{g_{m2\,on}-gm_{2\,off}}(C_{gd2,off} - C_{gd2,on})$

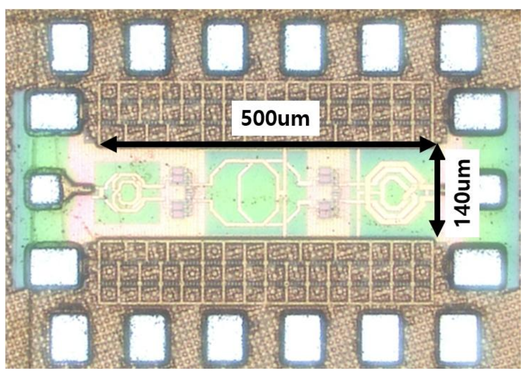
Proposed VGA Structure & Low phase variation condition

- Phase variation in conventional IIVGA is induced by the transistor of parasitic Cap (C_{gd}) and transconductance (g_m)
- The proposed VGA employs optimized phase control Cap (C_P) to achieve low phase variation across the gain control range

Measurement Result



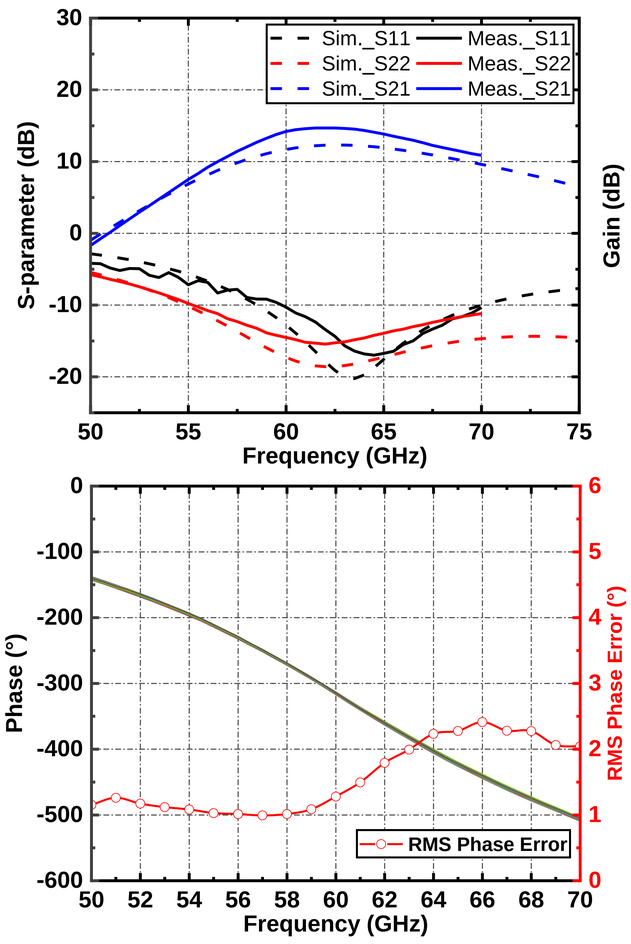
Measurement Setup



Chip Size: 0.72 * 490 um²

P_{DC}: 13 mW (@VDD 1 V)

Chip Microphotograph



Measurement Result (S-parameter, Gain Variation & Phase Variation at 24 dB Gain CTRL, Input Power Sweep)

- The VGA achieves a peak gain of 14.6 dB at 62.5 GHz
- The measured 3-dB bandwidth is 11 GHz
- The gain control range is 24 dB with 0.5 dB gain step
- The maximum RMS Gain Error and phase are 0.23 dB and 2.4°, respectively, over the frequency range of 57 to 70 GHz

Comparison Table & Conclusion

Reference	This work	RFIC 2019	IMS 2024	MWTL 2024	MWTL 2025
Topology	IIVGA CS	IIVGA CS	IIVGA CS	IIVGA CRS	CRS
Technology	28nm	65nm	65nm	65nm	65nm
Frequency (GHz)	57–70	20–43	57.1–70.7	53–66.5	27–31
Gain Control	Analog	Analog	Digital 10-bit	Digital 9-bit	Digital 7-bit
Max Gain (dB)	14.6	14.5	22.5	20	1.6
3-dB BW (GHz)	11	23	13.6	13.5	-
Gain Control Range (dB)	24	21.5	23.5	17.5	15.5
Gain Step (dB)	0.5	-	0.5	0.5	0.5
RMS Phase Error (°)	**<2.4**	<2	1.4-2.1	<2.6	0.46-1.58
RMS Gain Error (dB)	**<0.23**	-	0.05-0.09	<1.4	0.06-0.11
Power Dissipation (mW)	**13**	30.8	67.2	38.4	28
IP_{1dB} (dBm)	-12.8	-16.5	-9.5	-15.6	-8.1
Core Area (mm²)	**0.07**	0.34	0.15*	0.08	0.355

CS: Common Source. CRS: Current Steering.

- The Proposed VGA achieves low RMS gain error and phase error, small chip area and low power consumption

Acknowledgement

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