Simultaneous Switching Noise Compensator for Single-ended Voltage-mode Transmitters

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Abstract

This paper presents a simultaneous switching noise (SSN) compensator targeting multi-channel single-ended voltage mode widely used in memory and chiplet interfaces. The switched-capacitor based simultaneous switching current (SSC) compensator precisely nullifies the SSC profile, lowering the de-cap area cost and relieving the power consumption required for LDO bandwidth extension. Fabricated in 28nm CMOS, the prototype lower SSN by x0.23 in a 4 lane, 4Gb/s/lane simulation setup, with active area of 1776um^2/lane and energy-efficiency of 178fJ/b/lane.

Motivation

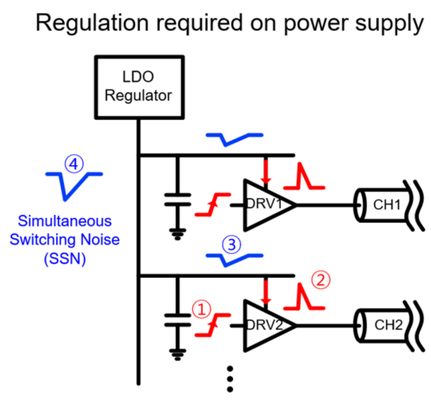

Fig 1. SSN in wide I/O

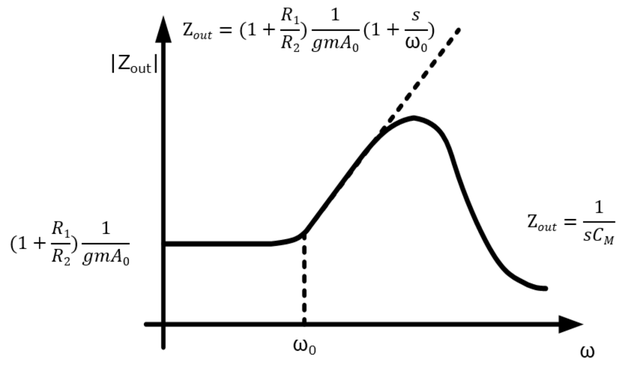

Fig 2. Mid-band Z_{11} hump in VDDQ

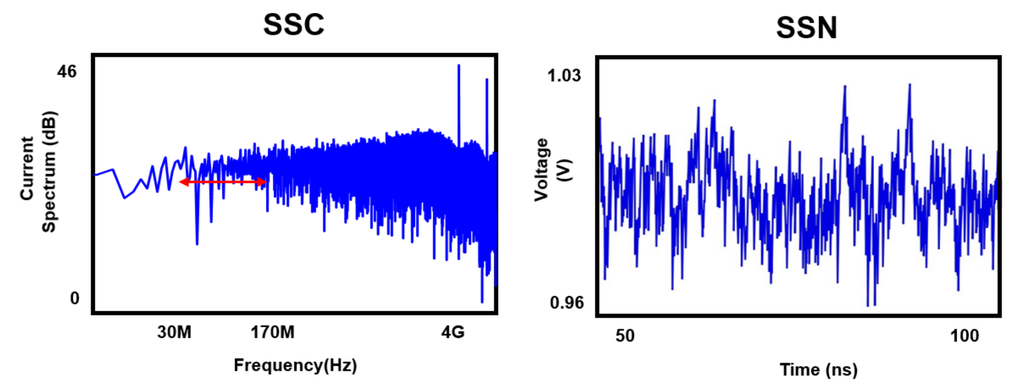

Fig 3. SSN resulting form SSC and Z_{11} of VDDQ

① **Low-frequency SSN: Regulated by LDO → High power required for BW extension ☹**
② **High-frequency SSN: Lowered by on-chip de-cap → Limited area budget ☹**
③ **Mid-frequency SSN: Cannot be fully resolved due to Z_{11} hump ☹**

➡ **SSC compensation: Lowers SSN w/ minimal de-cap cost and low power consumption ☺**

Proposed SSN Compensator

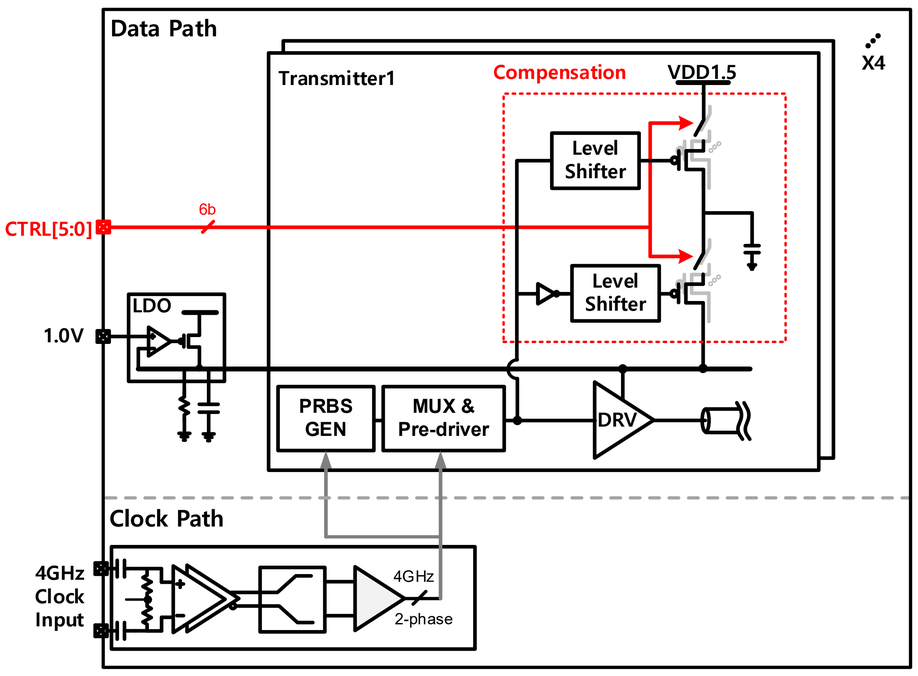

Fig 4. Overall architecture

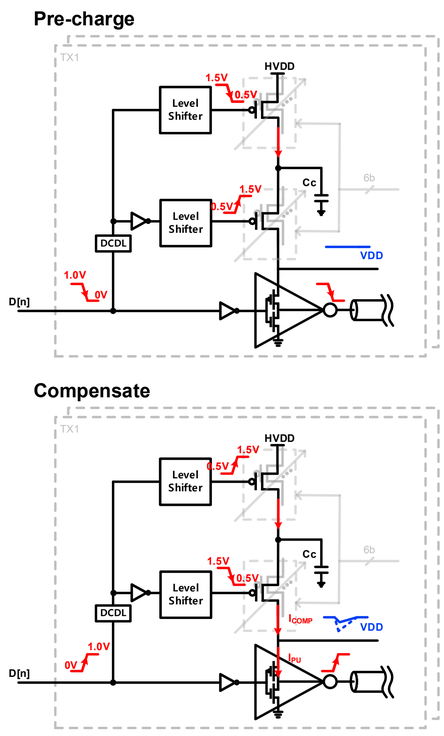

Fig 5. Switched-cap. operation

① **Switched-cap. based compensator: Compensates I_{PU} at every rising-edge**
② **SSC nullified to attenuate SSN of all bands ☺**
③ **DCDL & switch tuning is utilized to calibrate the compensator across PVT ☺**

Layout & Performance

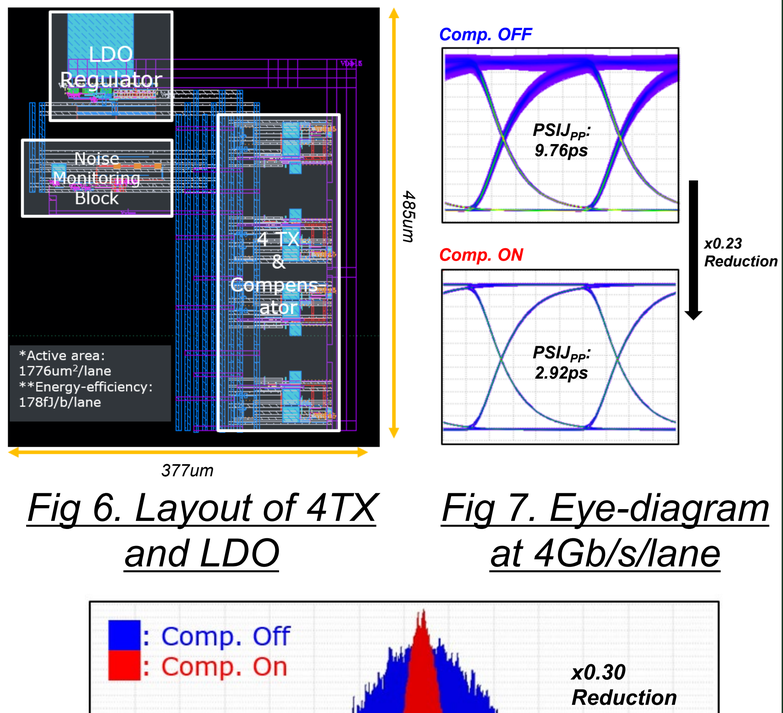

Fig 6. Layout of 4TX and LDO

Fig 7. Eye-diagram at 4Gb/s/lane

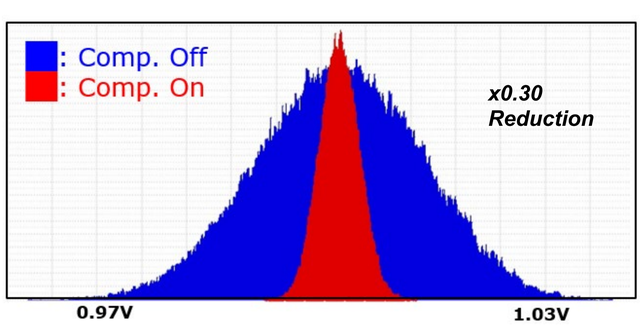

Fig 8. SSN comparison

Conclusion

- ✓ **Lower the de-cap area cost required to resolve high-frequency SSN. (20pF de-cap used to lower SSN by x0.23)**
- ✓ **Relieves the high power consumptions required to expand the LDO bandwidth. (Energy-efficiency of 178fJ/b/lane)**
- ✓ **Features flexibility to PVT variation with amplitude and delay tunability.**

Acknowledgements: The chip fabrication was supported by the IC Design Education Center(IDEC), Korea.