IDEC Chip Design Contest

Hardware-Efficient Parallel Pseudo-Random Ternary Sequence Generator

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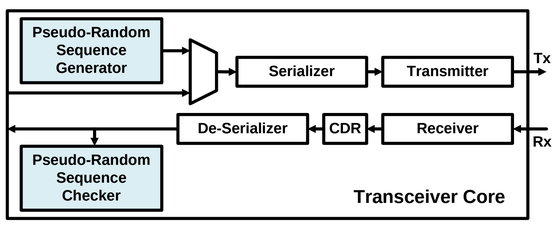
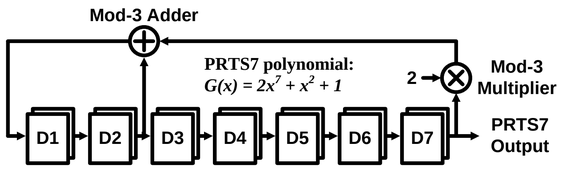
I. Introduction

- Pseudo-random ternary sequences (PRTS) are essential for high-speed serial interfaces using PAM-3 modulation, adopted in USB4 and GDDR7.



Overall architecture of a typical high-speed transceiver

- Conventional PRBS-based approaches require dedicated encoder/decoder and cannot generate standard-compliant polynomial-based PRTS patterns.
- Serial LFSR-based generation faces strict timing constraints at high data rates, motivating parallel generation schemes.



Serial LFSR-based PRTS7 generator

$$T = \begin{bmatrix} 0&1&0&0&0&0&2 \\ 1&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0 \\ 0&0&1&0&0&0&0 \\ 0&0&0&1&0&0&0 \\ 0&0&0&0&1&0&0 \\ 0&0&0&0&0&1&0 \end{bmatrix} \quad T^7 = \begin{bmatrix} 2&1&2&0&2&0&2 \\ 1&2&0&2&0&2&0 \\ 0&1&2&0&2&0&2 \\ 1&0&0&2&0&2&0 \\ 0&1&0&0&2&0&2 \\ 1&0&0&0&0&2&0 \\ 0&1&0&0&0&0&2 \end{bmatrix}$$

Transition matrix of PRTS7: basic matrix and exponentiated matrix for parallelization

- Transition matrix-based parallelization is effective for PRBS, but applying it to PRTS introduces challenges due to denser matrices and modulo-3 arithmetic.
- This work proposes a novel optimization methodology for efficient parallel PRTS generation with hardware-optimized design techniques.

II. Transition Matrix Optimization

A. Recursive and Reverse Recursive Substitution

- Recursive substitution restructures the matrix so non-zero entries shift rightward, reducing density of exponentiated matrices.
- Reverse recursive substitution (novel): folds out-of-range entries back and cancels overlapping terms under modulo-3 arithmetic.

4-Step Optimization Procedure:

- Step 1 (Expansion): Expand matrix via additional recursive substitution.
- Step 2 (Folding): Apply reverse recursive substitution to fold entries into target width.
- Step 3 (Element Minimization): Merge candidates using modulo-3 cancellation.
- Step 4 (Selective Row Replacement): Replace rows with fewer non-zero elements.

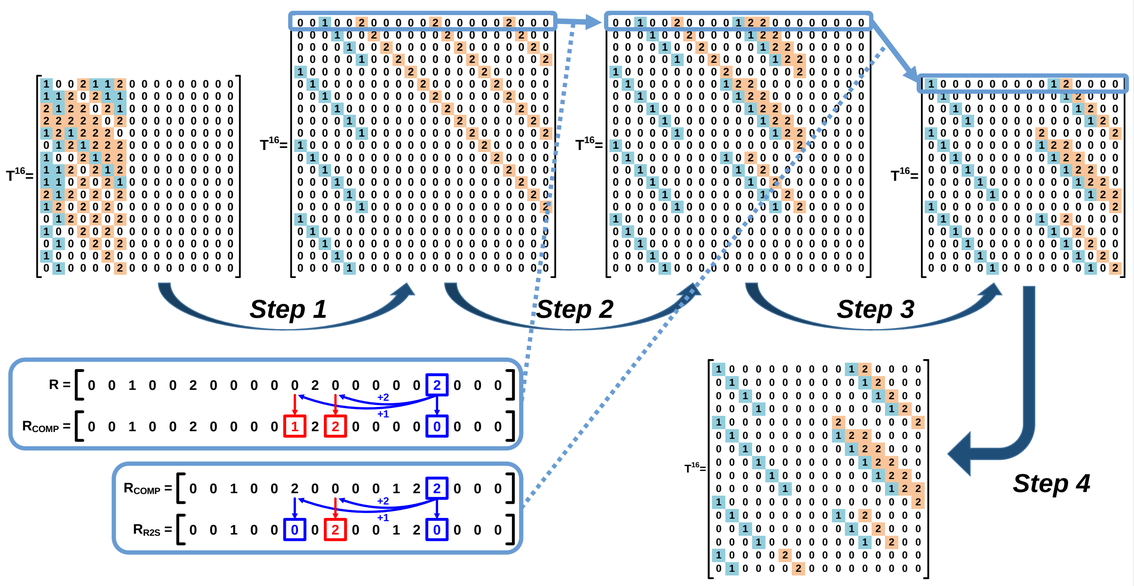
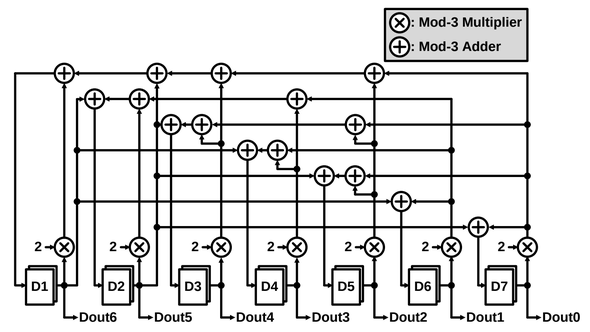


Table 1. The Number of Adders and Maximum Fan-Out across Optimization Steps

Length	PRTS7								PRTS19							
Parallel-way	16-way		32-way		64-way		128-way		16-way		32-way		64-way		128-way	
Count	Adder	F.O.	Adder	F.O.	Adder	F.O.	Adder	F.O.	Adder	F.O.	Adder	F.O.	Adder	F.O.	Adder	F.O.
Baseline	58	12	134	25	242	45	465	87	72	9	256	22	729	49	1589	96
Step 0	-	-	97	8	148	6	451	12	-	-	-	-	373	13	1242	31
Step 1-3	36	7	85	8	148	6	324	7	-	-	204	21	366	13	759	18
Step 4	34	7	84	8	137	9	281	12	-	-	-	-	-	-	753	17

III. Modulo-3 Operators and Hardware Optimization



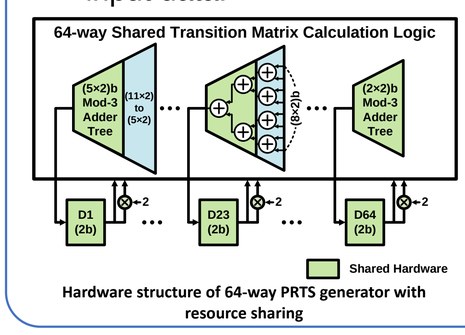
Hardware implementation of the transition matrix for 7-way parallel PRTS7 generation

A. Modulo-3 Operator Optimization

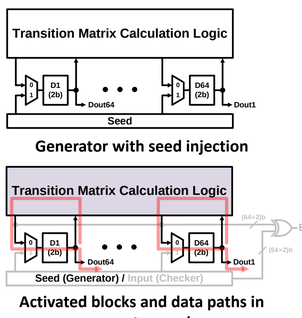
- Multiplication by 2: Implemented as MSB-LSB swap (zero logic gates).
- LUT-based adder: 28.9% area, 46.3% power, 12.1% delay reduction vs. baseline.
- N-input adder tree: Up to 53.5% delay improvement for deeper trees.

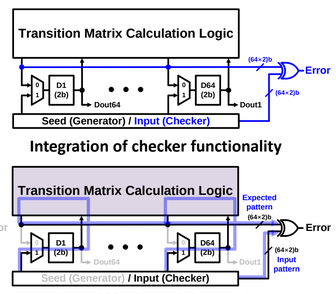
B. Hardware Sharing & Checker Integration

- Flip-flops fully shared between PRTS7 and PRTS19; adder trees partially shared via multiplexing.
- 26-32% area reduction compared to separate implementations.
- Checker reuses generator hardware by disabling feedback path and loading input data.



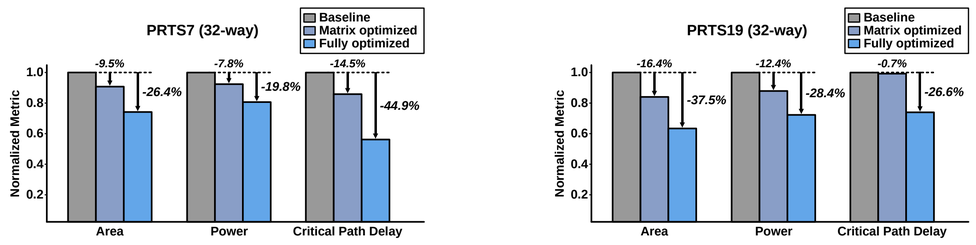
Hardware structure of 64-way PRTS generator with resource sharing





IV. Implementation and Measurement Results

A. Optimization Impact (32-way, 40 Gbps)



B. Test Chip Measurements (28-nm FDSOI)

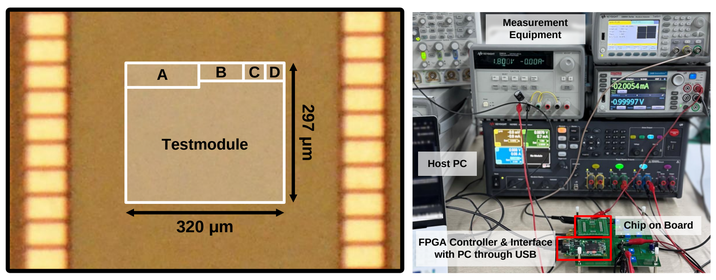


Table 2. Measured Power Consumption for 40Gbps in Generation Mode

Parallel-way	Operating Frequency	Power	
		PRTS7	PRTS19
16	1.6 GHz	1.98 mW	2.07 mW
32	800 MHz	1.19 mW	1.20 mW
64	400 MHz	1.11 mW	1.32 mW
128	200 MHz	1.27 mW	1.47 mW

Table 3. Measured Power Consumption for 40Gbps in Checker Mode

Parallel-way	Operating Frequency	Power	
		PRTS7	PRTS19
16	1.6 GHz	2.31 mW	2.44 mW
32	800 MHz	1.37 mW	1.43 mW
64	400 MHz	1.29 mW	1.53 mW
128	200 MHz	1.47 mW	1.73 mW

C. Comparison with Prior Works

	This work	JSSC'21	TCAS-II'24	TCAS-I'25	TCAS-I'25
Technology	**28nm CMOS**	28nm CMOS	28nm CMOS	65nm CMOS	22nm CMOS
Pattern generate scheme	**PRTS native generator**	PRBS generator + Encoder			
Data rate per lane	**40 Gb/s**	30 Gb/s	12 Gb/s	22.5 Gb/s	36 Gb/s
Degree of Parallelization	**32**	8×3	8×3	8×3	2×3
Number of DFFs	**64**	24	24	24	6
Operating frequency of Generator	**800 MHz**	1.25 GHz	500 MHz	937.5 MHz	6 GHz
Operating frequency of Encoder	-	10 GHz	1 GHz	7.5 GHz	12 GHz
Supported PRTS Patterns	**PRTS7/ PRTS19**	PRBS-based Ternary			
Supply voltage	**1.0 V**	0.6 V	1.0 V	0.6 V	1.0 V
Energy per bit (Generator+Encoder)	**0.030 pJ/b**	-	0.075 pJ/b	0.075 pJ/b	0.36 pJ/b
Area (Generator+Encoder)	**0.0017 mm²**	-	0.0044 mm²	-	-

V. Conclusion

- A novel transition matrix optimization and low-complexity modulo-3 operators for parallel PRTS generation.
- Unified PRTS7/PRTS19 core with integrated checker, fully compliant with USB4.
- 28-nm FDSOI test chip: 166.2 Gb/s peak, 0.030 pJ/b, < 0.006 mm²

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