IDEC Chip Design Contest

A 60-70 GHz Vector Sum Phase Shifter in 65nm CMOS Technology

Hyeong Jin An and Chul Woo Byeon

Department of Electronic and Electrical Engineering, Dankook University, Gyeonggi-do, Korea

Introduction

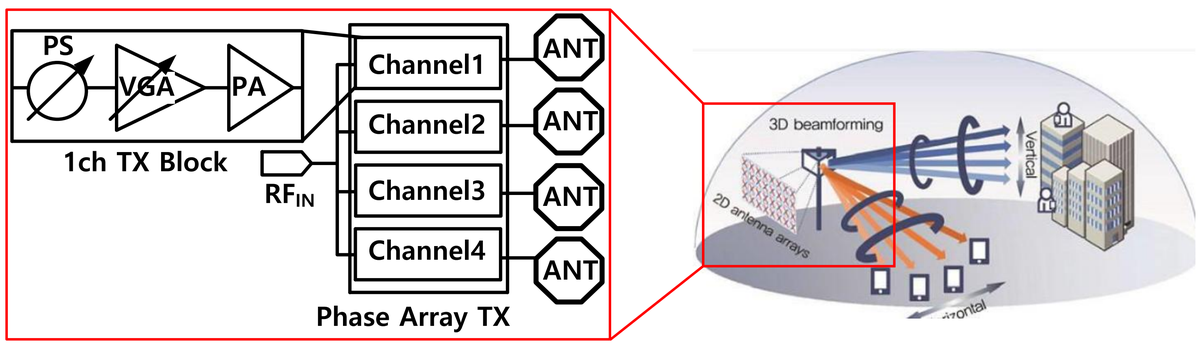

Fig 1. Phased-arrays and beamforming technique for wireless systems

- The phase shifter is a key component in the transmitter that enables beam forming through phase control
- Transmitter for 60 GHz beamforming
  ⇒ Accurate beam steering through phase control

Proposed Vector Sum Phase Shifter (VSPS)

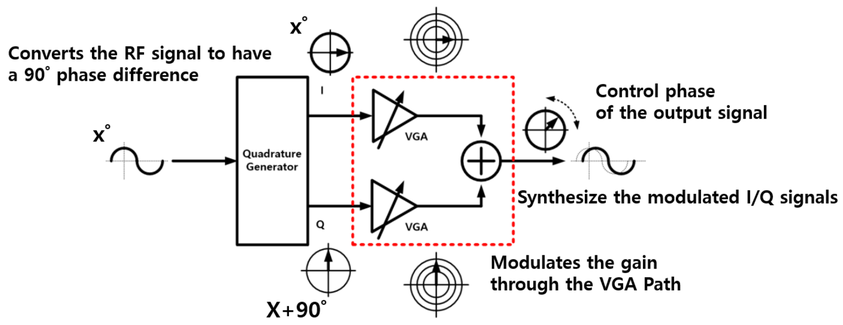

Fig 2. Conventional Vector Sum Phase Shifter (VSPS)

- The phase of the output signal is controlled by synthesizing the modulated I/Q signals
- I/Q signals using vector sum require minimizing phase error and gain error for accurate synthesis of the modulated I/Q signals

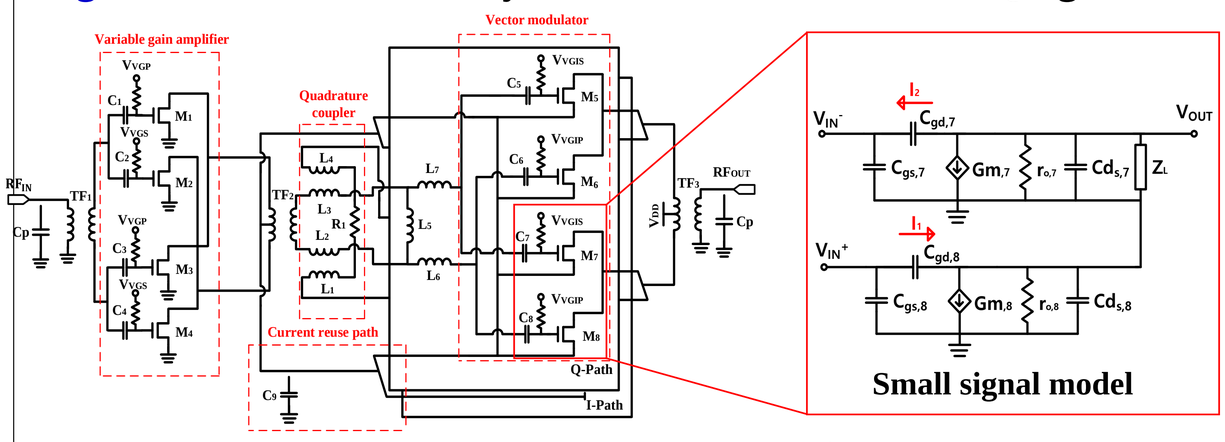

Fig 3. Proposed Vector Sum Phase Shifter (VSPS)

- Impedance invariant variable gain amplifier (IIVGA)
  : When a constant current condition, impedance invariance

Phase Equation by small signal model

$$A_{v,IIVGA} = -\frac{((gm_8 - gm_7)-(jwC_{gd,8} - jwC_{gd,7}))}{(jwC_{gd,8} + jwC_{gd,7} + jwC_{ds,8} + jwC_{ds,7} + Y_{ds,8} + Y_{ds,7} + \frac{1}{jwL_L})}$$

$$\rightarrow \Delta A_{v,IIVGA} \approx (\Delta gm_8 - \Delta gm_7) - (jwC_{gd,8} - jwC_{gd,7})$$

$$\rightarrow \Delta\varphi_{IIVGA} \approx \tan^{-1}(-\frac{wC_{gd,8} - jwC_{gd,7}}{\Delta gm_8 - \Delta gm_7})$$

If, $wC_{gd,8} \cong wC_{gd,7} \rightarrow \Delta\varphi_{IIVGA} \approx 0$

⇒ reduced phase variation (by eliminating Cgd (Parasitic Cap.))

- Quadrature coupler (QC)
  : Provide orthogonal signals for the I and Q-path
- Current reuse path
  : As the sources of M_5 - M_8 and the center tap of the TF_2 are directly connected, the dc current can be reused

Measurement Result

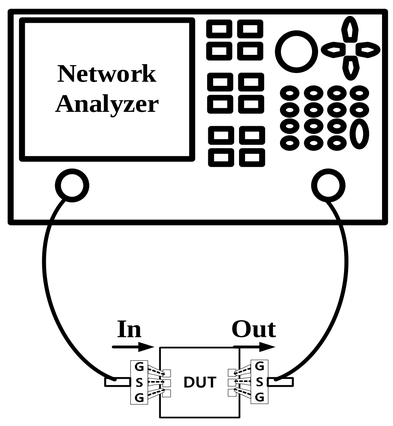

Fig 4. Measurement Setup

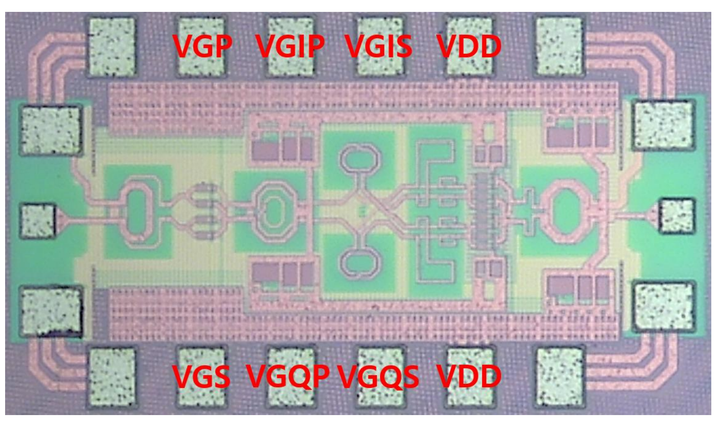

Fig 5. Fabricated VSPS Microphotograph

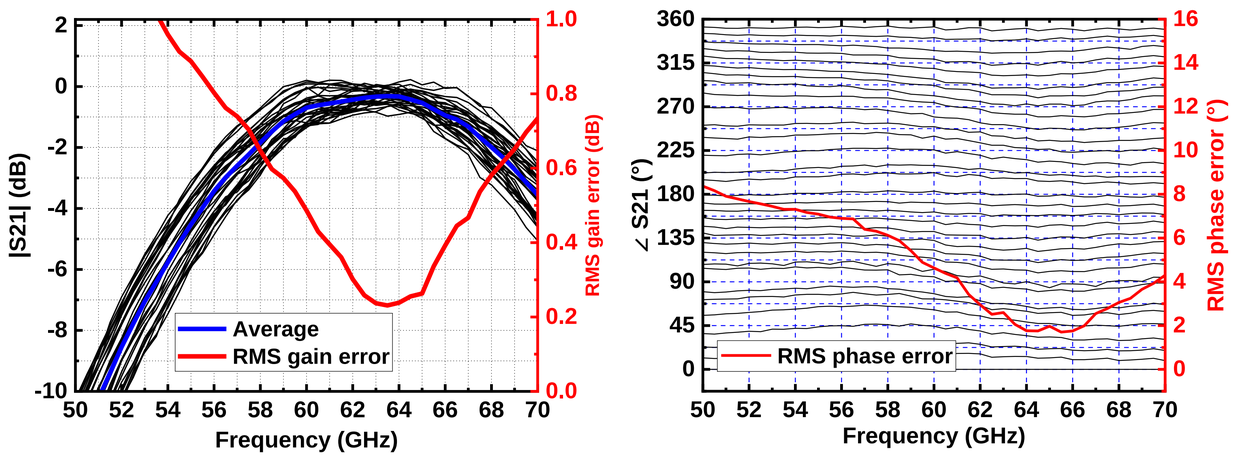

Fig 6. Measured gain and phase variation with RMS gain and phase error at 360° phase control (@ 11.25° step)

CMOS 65nm Technology	Simulation	Measurement
Frequency (GHz)	57 – 71	60 – 70
Phase Shift Range (°)	360	
Phase Resolution (bits)	5	
Gain (dB)	-0.3 ~ -3.9	0 ~ - 0.3
3-dB BW (dB)	12.5	13.5
RMS Phase Error (°)	0.57 – 1.97	1.7 – 4.63
RMS Gain Error (dB)	0.1 – 0.25	0.23 – 0.73
IP1dB	-9.71 (@64GHz)	-9.5 (@64GHz)
P_{DC} (mW)	9.48	10
Chip Size (mm^2)	0.171	

- The 3-dB bandwidth is achieved wide bandwidth of 13.5 GHz
- The measured RMS phase error is 1.7 – 4.63° over the 57-71 GHz
- The measured RMS gain error is 0.23 – 0.73 dB over the 57-71 GHz

Comparison Table & Conclusion

Reference	This work	TMTT 2023	TMTT 2021	TMTT 2020	ISCAS 2022
Technology	65nm	65nm	65nm	65nm	65nm
Quadrature Generation	TFQC	RL PPF*	TFQC	Hybrid QC	TFQC
Vector Modulation	IIVGA	Gilbert-Cell	IIVGA	IIVGA	Gilbert-Cell
Frequency (GHz)	60 – 70	56.8 – 64.1	50 – 64	51 – 66.3	27 – 34, 55 - 63
Phase Shift Range (°)	360	360	360	360	360
Phase Resolution (Bits)	5	5	6	5	5
Gain (dB)	0 ~ - 0.3	<8	<-5.8	-3.8(peak)	-0.2 - -5.8
3-dB BW (dB)	13.5	7.3	14	15.3	7(27 - 34) 8(55 - 63)
RMS Phase Error (°)	1.7 – 4.63	0.36 – 1.44	<3.3	3 – 7	<3.07 (Sim)
RMS Gain Error (dB)	0.2 – 0.73	0.13 – 0.26	<0.5	0.25 – 0.72	<1.91 (Sim)
IP1dB (dBm)	-9.5	-14.6	N/A	-0.23	-8.7
P_{DC} (mW)	10	14.5	18	5	32
Chip Size (mm^2)	0.171	0.55	0.403	**0.403**	0.314

*Poly Phase Filter

- The proposed VSPS achieved a acceptable RMS error and bandwidth with lower power consumption and a small chip area compared to other papers.

Acknowledgement

This paper was supported by Korea Institute for Advancement of Technology (KIAT) grant funded by the Korea Government (MOTIE) (RS-2025-02214408, HRD Program for Industrial Innovation)