

## A 4.8 – 36.0 GHz Inverter-based Variable-gain Amplifier With PMOS Varistor in 28-nm Bulk CMOS

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### Introduction

#### ■ Motivation of multi-band operation

- Support multiple wireless protocols within a single architecture, enabling flexible and efficient spectrum usage.
- Reduced system cost, area, and power by consolidating functionality.

#### ■ The necessity of a wideband variable-gain amplifier (VGA)

- Compensates for signal strength variation across different frequency bands.

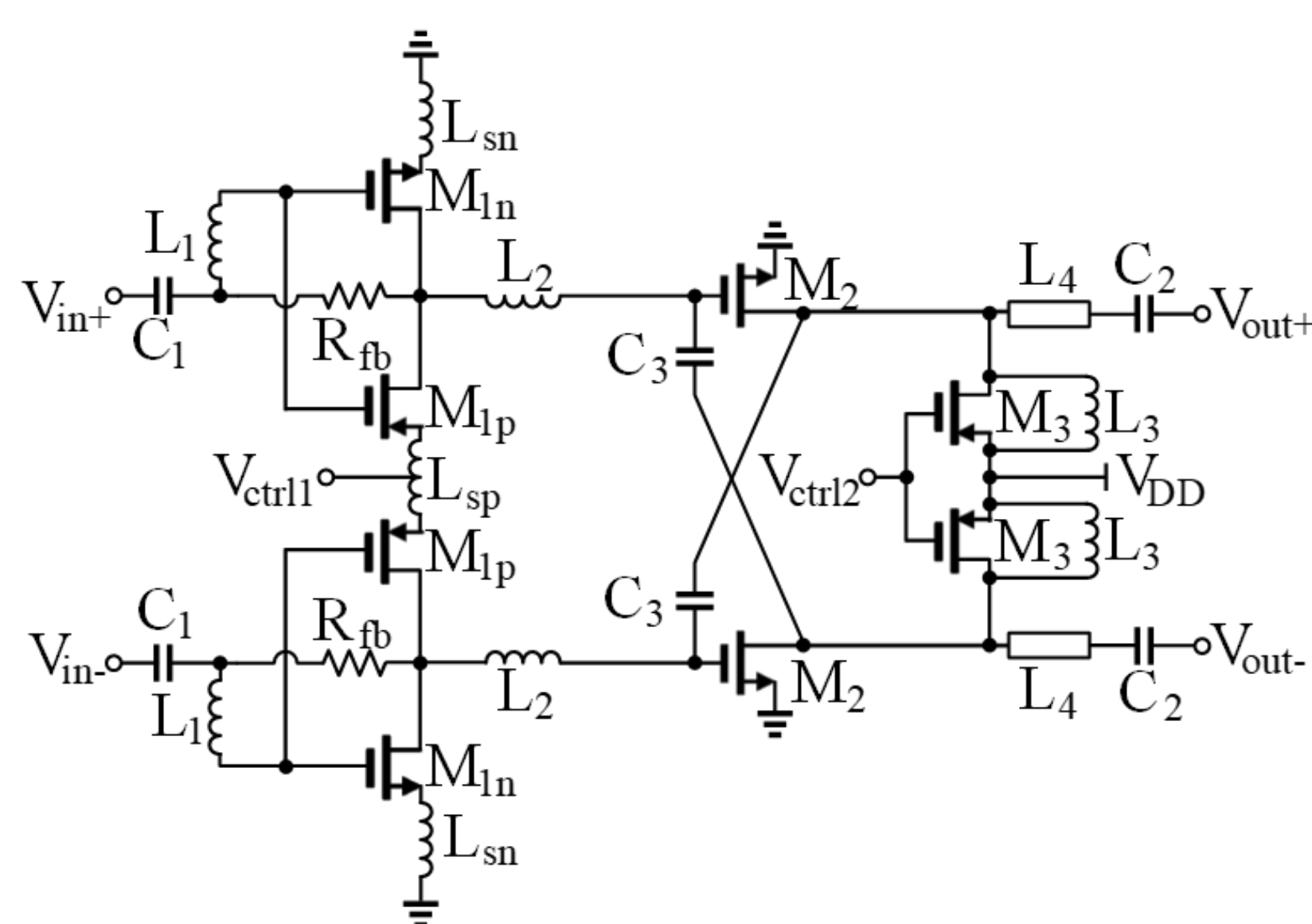
### Design

#### ■ Transconductance tuning by concurrent current steering

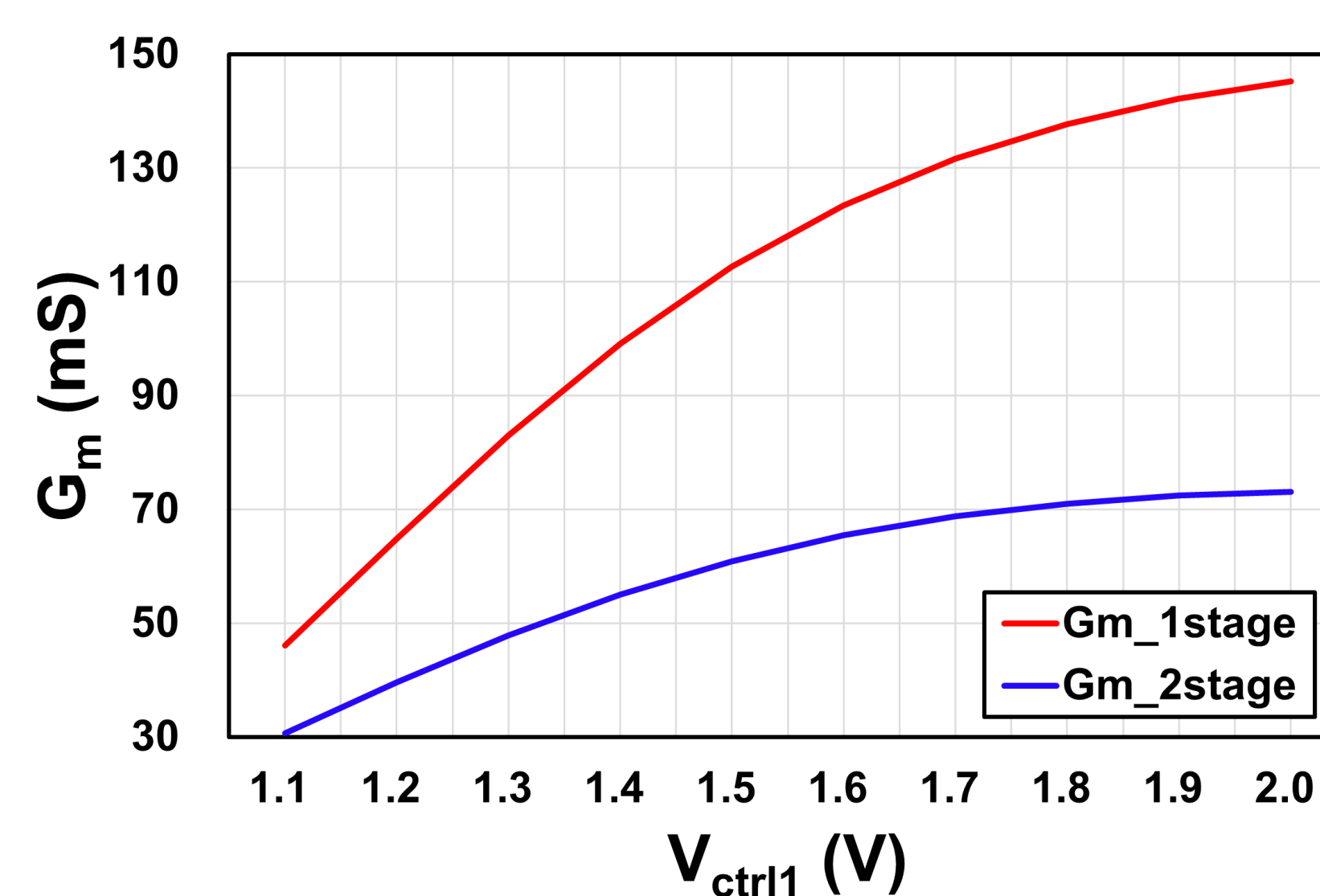
- $V_{ctrl1}$  simultaneously biases all active devices without inter-stage DC-block.
- $G_{m,1stage}$  and  $G_{m,2stage}$  by  $V_{ctrl1}$  vary with the same polarities, effective gain tuning is achieved.

#### ■ Load impedance tuning by PMOS varistor

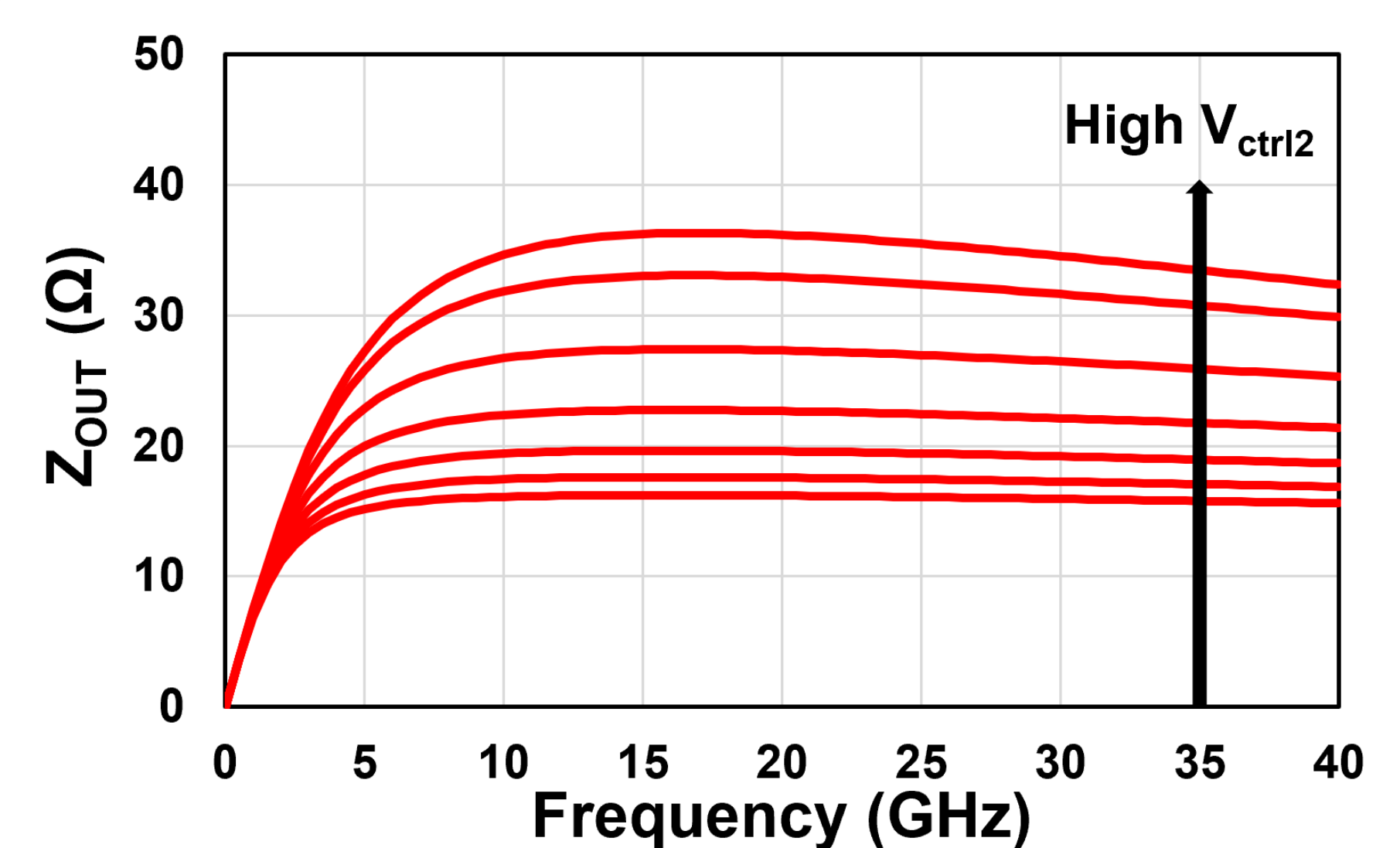
- PMOS varistor in parallel with  $L_3$  expands the gain tuning range by modulating the output impedance with  $V_{ctrl2}$ .
- $L_3$  eliminates dc drops to maximize headroom and resonates with parasitic  $C_{ds}$  to maintain high impedance path.



<VGA Schematic>



<Simulated  $G_M$  by  $V_{ctrl1}$ >

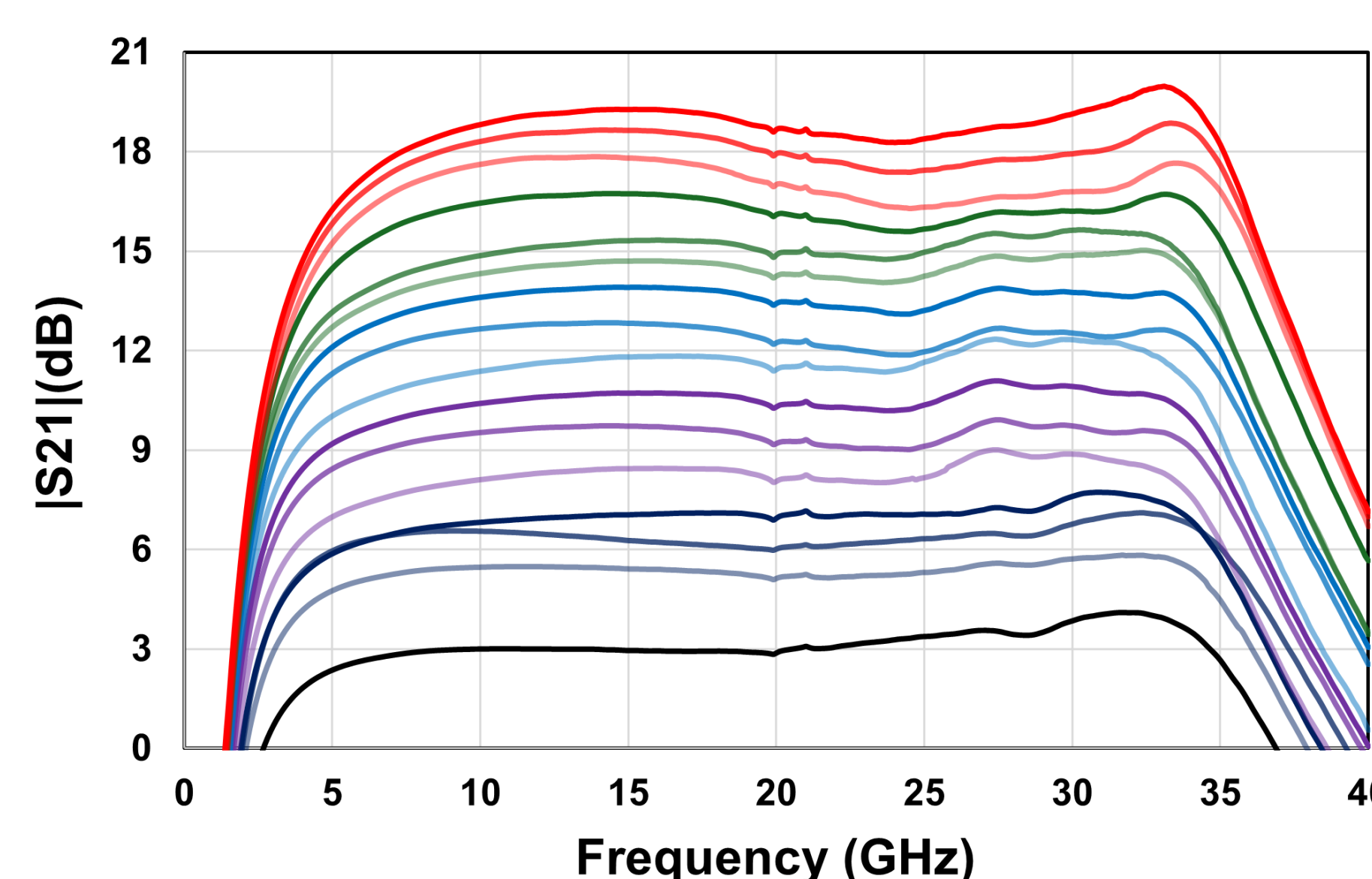
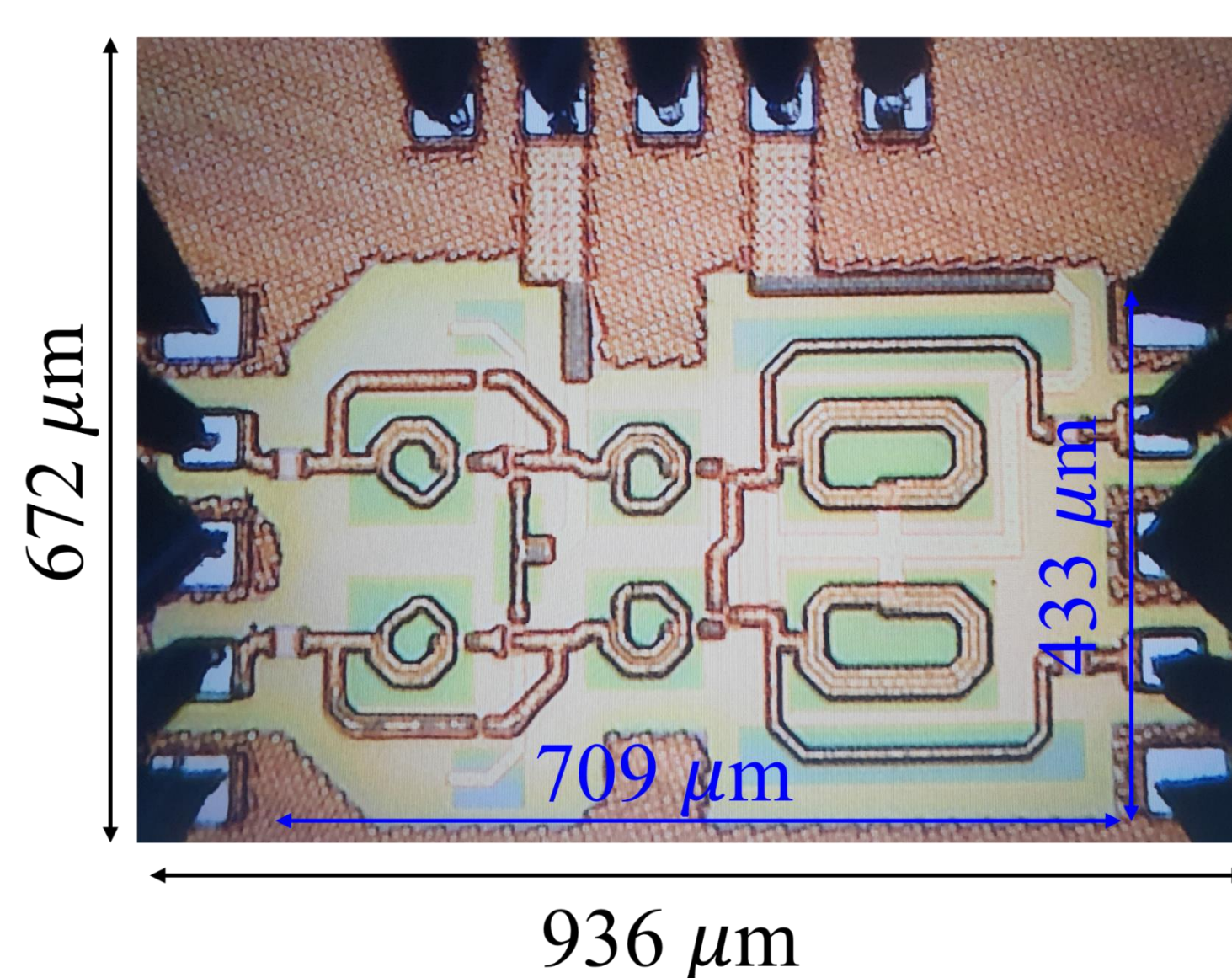


< Simulated  $Z_{OUT}$  by  $V_{ctrl2}$  >

### Results

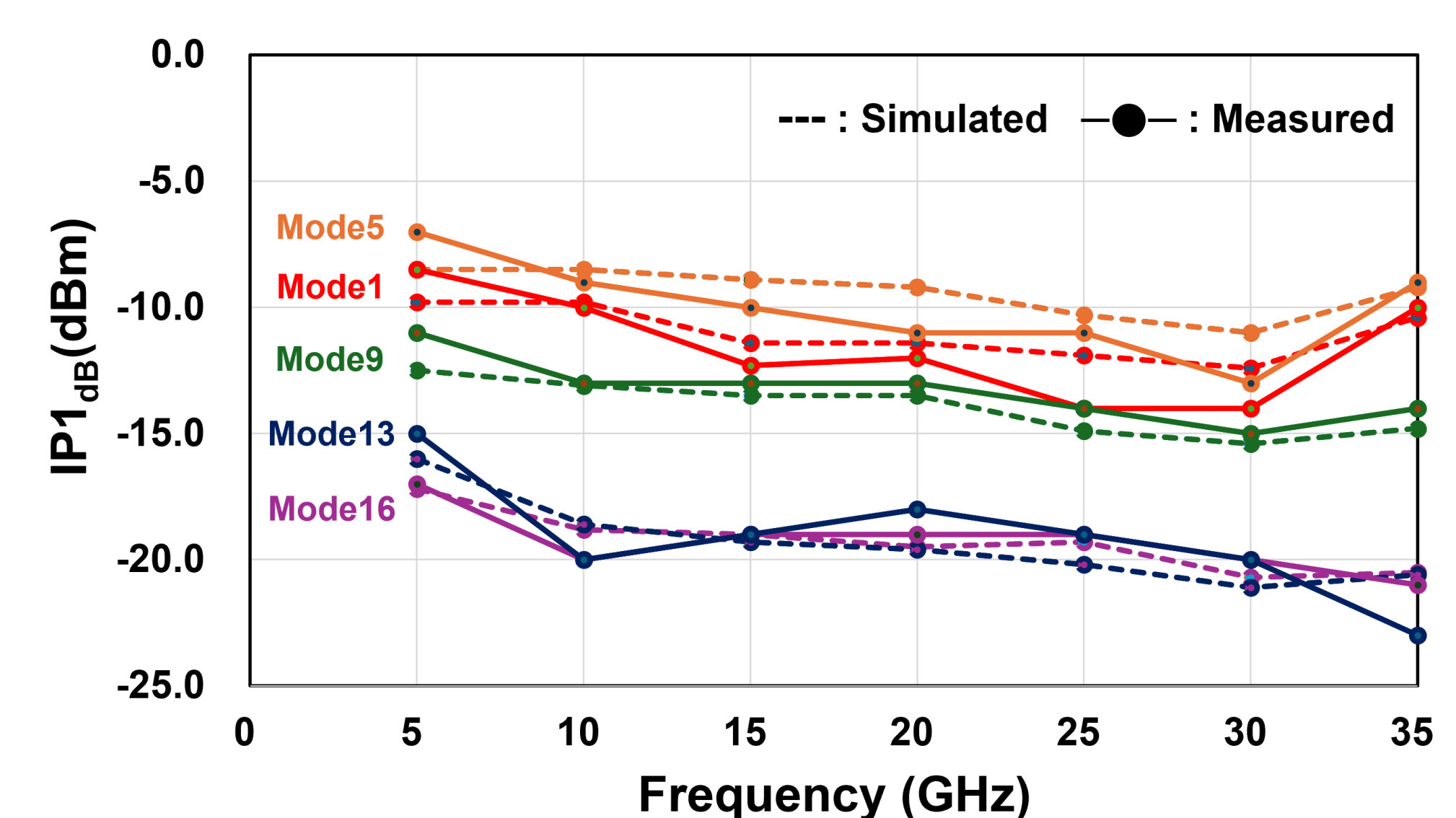
#### ■ Chip photograph & measured S-parameters

- Peak  $S_{21}$  : 19.9 dB
- 3-dB BW : 31.2 GHz (4.8–36.0 GHz)



#### ■ Linearity & NF measurement

- $IP_{1dB}$  : -23.0 - -15.0 dBm
- NF : 4.0 ~ 6.2 dB



### Conclusion

- We have developed a wideband inverter-based VGA with PMOS varistor in a 28-nm CMOS process.
- The VGA demonstrates 16.9 dB gain tuning range and maintains wide 3-dB BW with 4.8–36.0 GHz.
- It consumes 24–65 mW of DC power across all gain modes.

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea