IDEC Chip Design Contest

A Pattern-Dependent Pulse Filtering Technique for Low-Jitter Injection-Locked CDR in 28-nm CMOS

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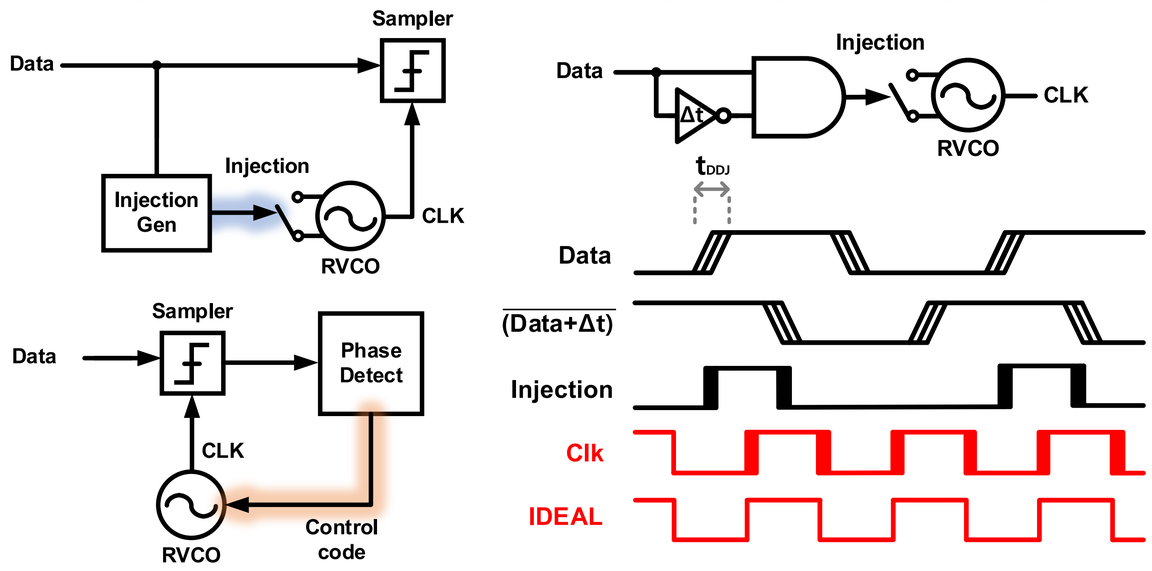
Introduction

◆ Motivation of Injection-Locked CDR (ILCDR)

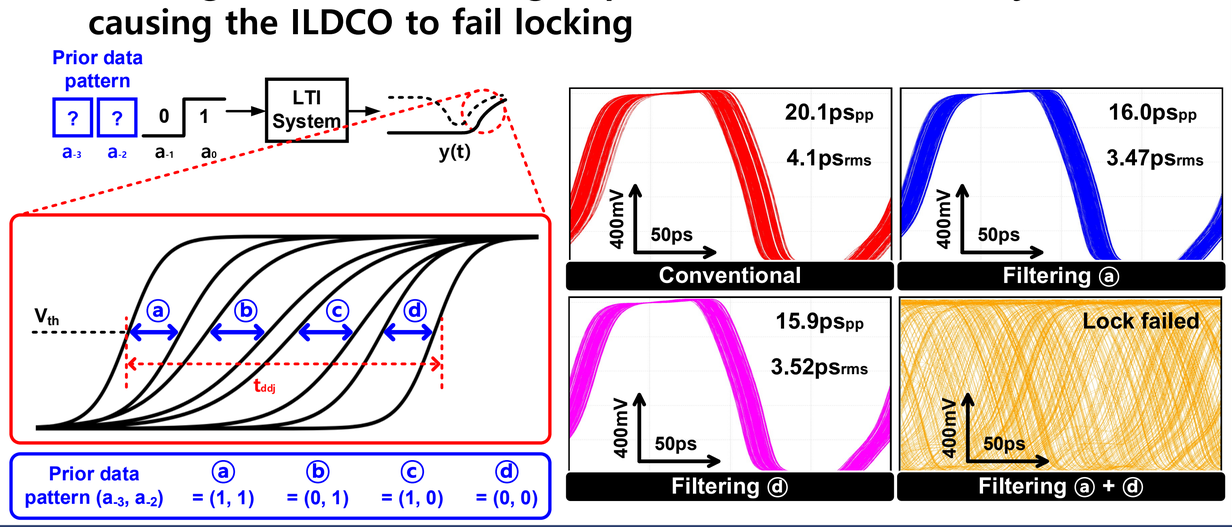
- ✓ ILCDR offers fast lock time, high JTOL, and wide bandwidth, making it ideal for low power burst-mode.
- ✓ Conventional ILCDR transferring data-dependent jitter (DDJ) directly to the recovered clock and degrading its timing margin.



Pattern-Dependent Pulse Filtering Technique

◆ Proposed PDPF technique

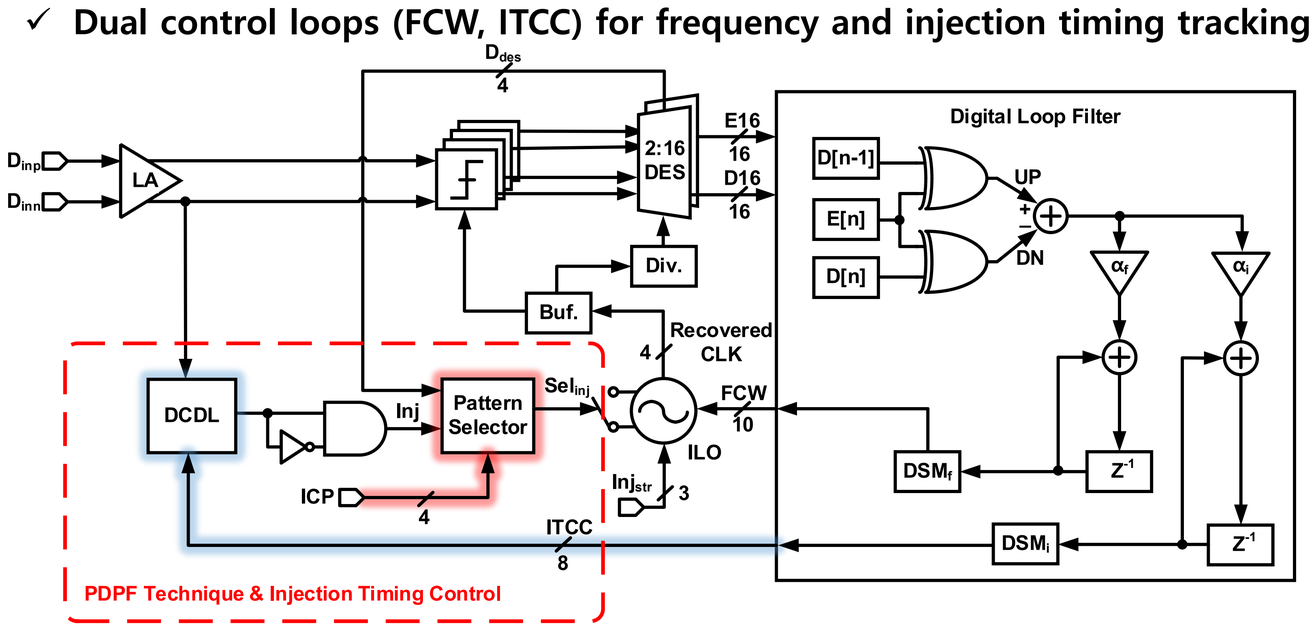
- ✓ Classify data transitions into 4 groups (ⓐ, ⓑ, ⓒ, ⓓ) based on 2-bit prior pattern
- ✓ Selectively filter injection pulses in the range that contribute the largest DDJ
- ✓ Filtering more than two groups leaves insufficient injection rate, causing the ILDCO to fail locking



Overall Block Diagram & Circuit Implementation

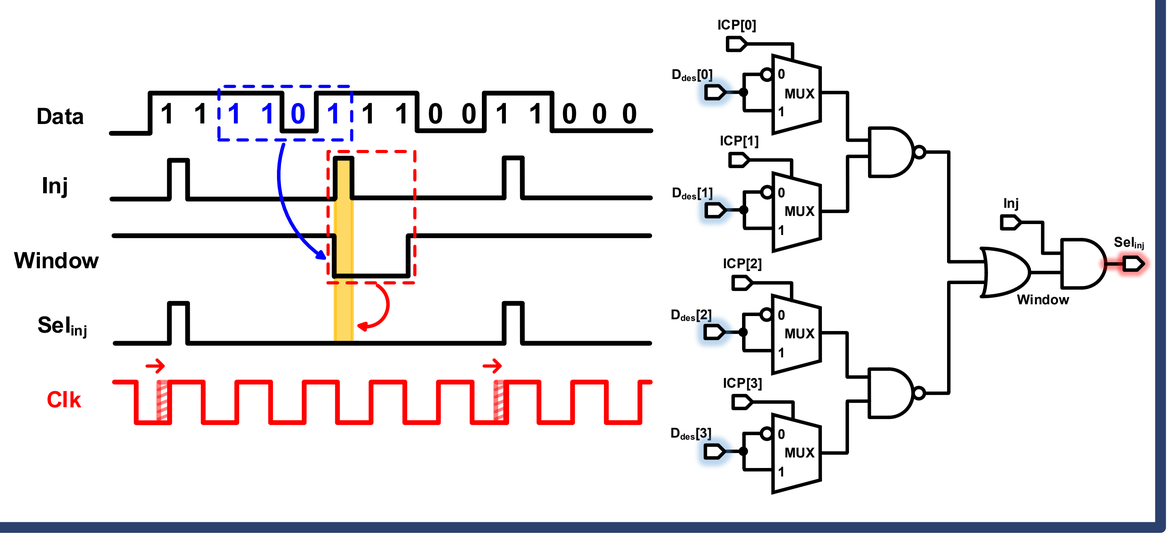
◆ Injection-Locked CDR with Pattern-Dependent Pulse Filtering Technique

- ✓ ILDCO generates 5-GHz clock for half-rate recovery, injection controlled by Sel_{inj}
- ✓ Dual control loops (FCW, ITCC) for frequency and injection timing tracking



◆ Pattern Selector (PDPF core)

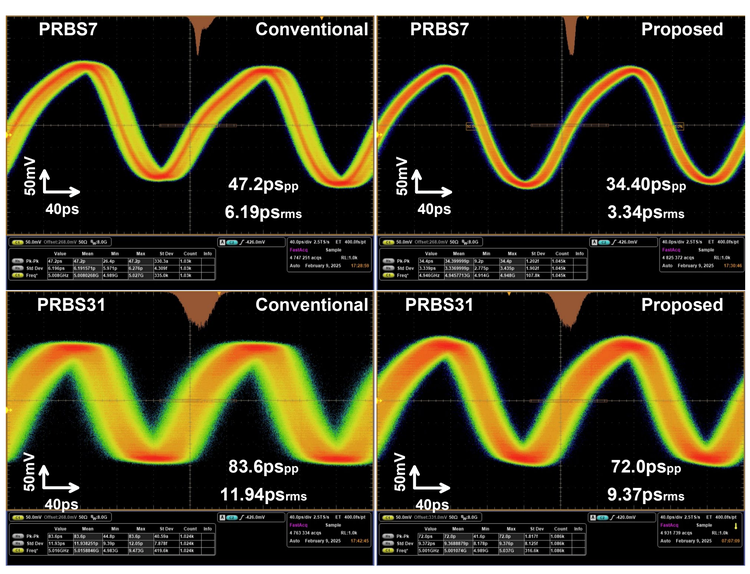
- ✓ Detects 4-bit prior data pattern from deserialized data
- ✓ ICP-controlled MUX selects target pattern
- ✓ Enables selective filtering of high-DDJ injection pulses

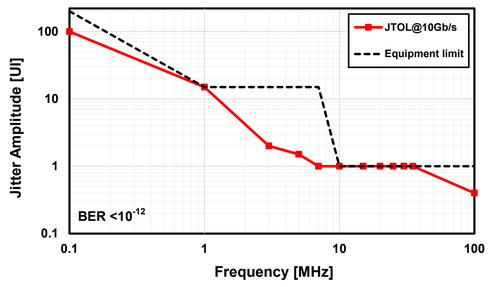


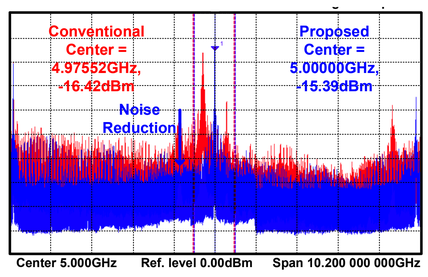
Measurement Results

◆ Measured jitter & noise reduction with PDPF

- ✓ Jitter histograms measured for PRBS7 and PRBS31, with and without PDPF
- ✓ Achieves JTOL of 1.0 UI_{pp}@35MHz and 0.4UI_{pp}@100MHz under BER < 10^{-12}
- ✓ Dual control loop enables accurate frequency tracking, while PDPF reduces the overall clock noise



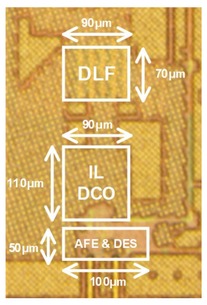


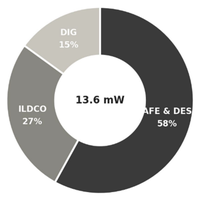


Chip Photo & Performance Comparison

◆ Chip photomicrograph & performance comparison

- ✓ Fabricated in Samsung 28-nm CMOS technology
- ✓ Active area: 0.021mm^2, Power efficiency : 1.36pJ/b





	JSSC'15 [1]	JSSC'16 [2]	JSSC'19 [3]	ESSERC'25 [4]	This Work
Technology [nm]	90	28	28	28	**28**
Architecture	Full rate	Half rate	Half rate	Quarter rate	**Half rate**
Oscillator Type	GVCO	ILO	ILO	ILO	**ILO**
Jitter Reduction Technique	Injection Rate Control	-	Injection Timing Optimization	Jitter-Filtering Retimer	**Pattern-Dependent Pulse Filtering**
Supply Voltage [V]	1.2	0.9	0.9	0.9	**1.0**
Data Rate [Gb/s]	2.2	12	10	20	**10**
Power [mW]	6.1	22.9	12.8	58.6	**13.6**
Energy Efficiency [pJ/bit]	2.77	1.9	1.28	2.96	**1.36**
Bit Error Rate	< 10^{-12}	< 10^{-9}	< 10^{-12}	< 10^{-12}	**< 10^{-12}**
Jitter Tolerance	1.0 UI_{pp} @ 4 MHz	1.0 UI_{pp} @ 120 MHz	1.0 UI_{pp} @ 31 MHz	1.0 UI_{pp} @ 173 MHz	**1.0 UI_{pp} @ 35 MHz**
Clock RMS Jitter [ps]	3.9	-	3.59	-	**3.34**

◆ Acknowledgement

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◆ References

[1] W.-S. Choi, JSSC 2015
[2] T. Masuda, JSSC 2016
[3] M.-S. Choo, JSSC 2019
[4] I. Kim, ESSERC 2025

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