IDEC Chip Design Contest

A High-Isolation Compact W-Band Switched-Neutralized SPDT Switch

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▪ Introduction

• High-isolation W-band SPDT switch • Switched neutralization technique for isolation enhancement • 28-nm CMOS FD-SOI

▪ Main Subject

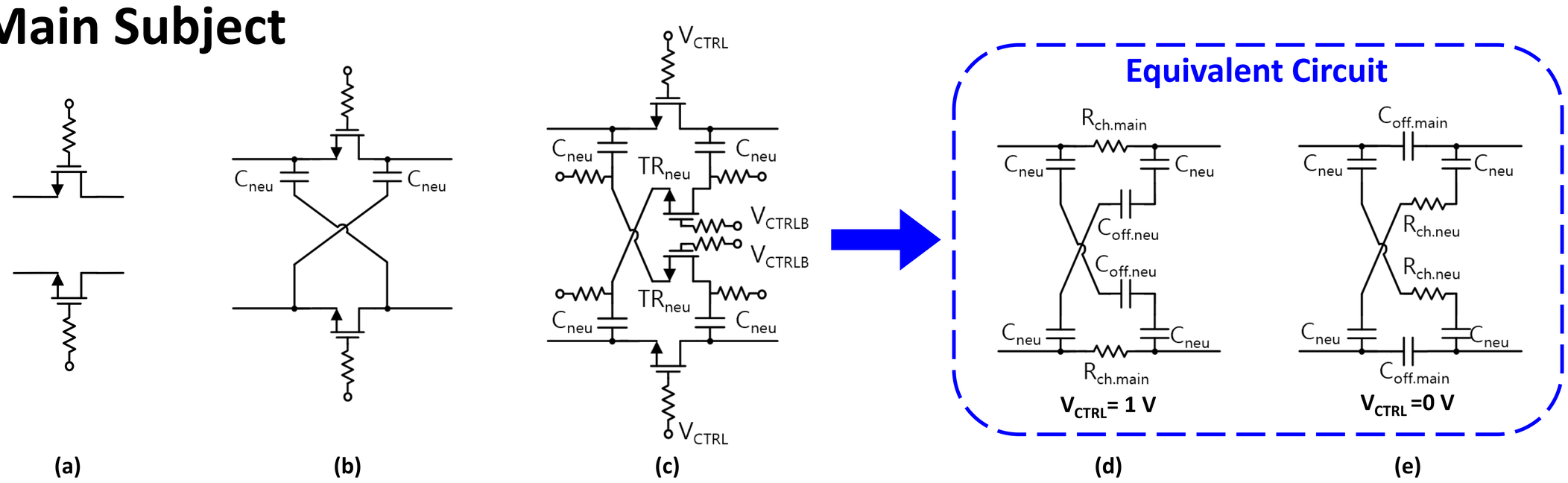

Fig. 1. series SPST switches: (a) conventional, (b) with neutral capacitor, (c) proposed neutralization network and its equivalent circuits; (d) V_{CTRL}= 1 V, (e) V_{CTRL}= 0 V.

- Neutralization network with capacitors and a transistor (TR_{neu})
- Isolation mode: TR_{neu} on → leakage cancellation via anti-phase signal
- Bypass mode, TR_{neu} off → Reduced leakage through the network.

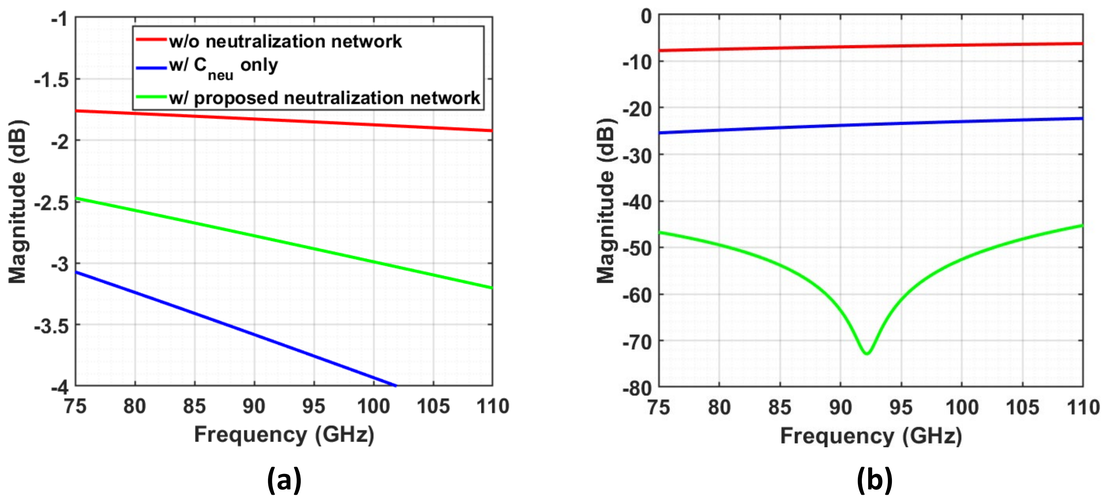

Fig. 2. Simulated SPST performance across neutralization networks: (a) IL, (b) isolation

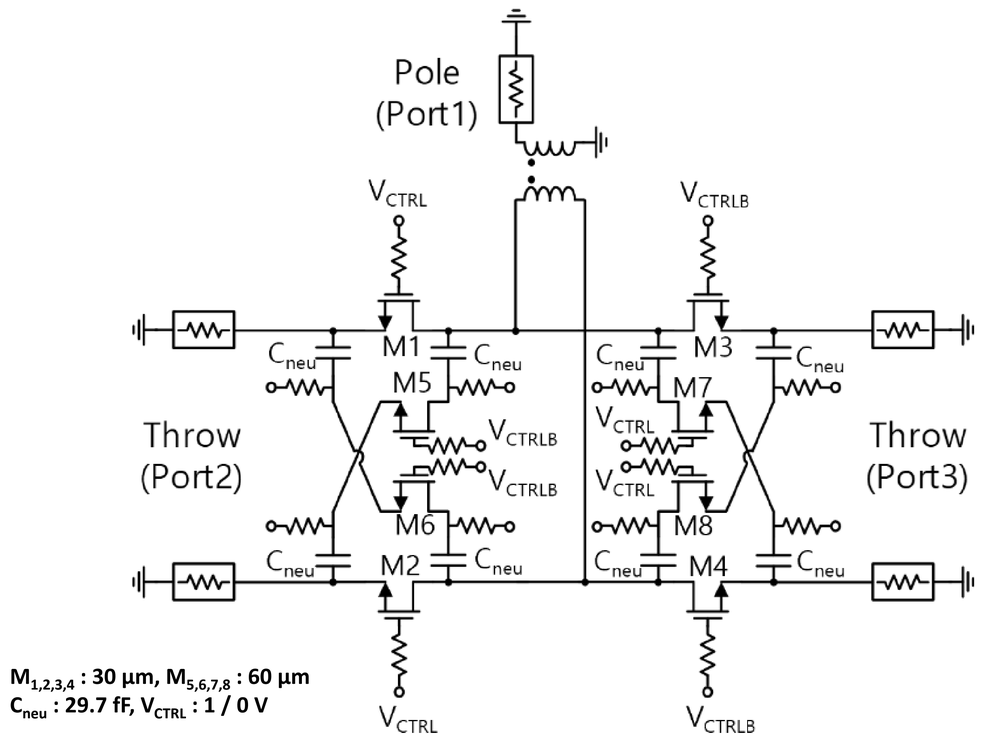

Fig. 3. Schematic of the proposed high-isolation switched-neutralized SPDT switch.

▪ Conclusion

- High-isolation W-band SPDT switch demonstration
- Effective isolation enhancement via switched neutralization
- > 26 dB isolation across the entire band
- Thin Mx layer routing not accurately captured in EM simulation

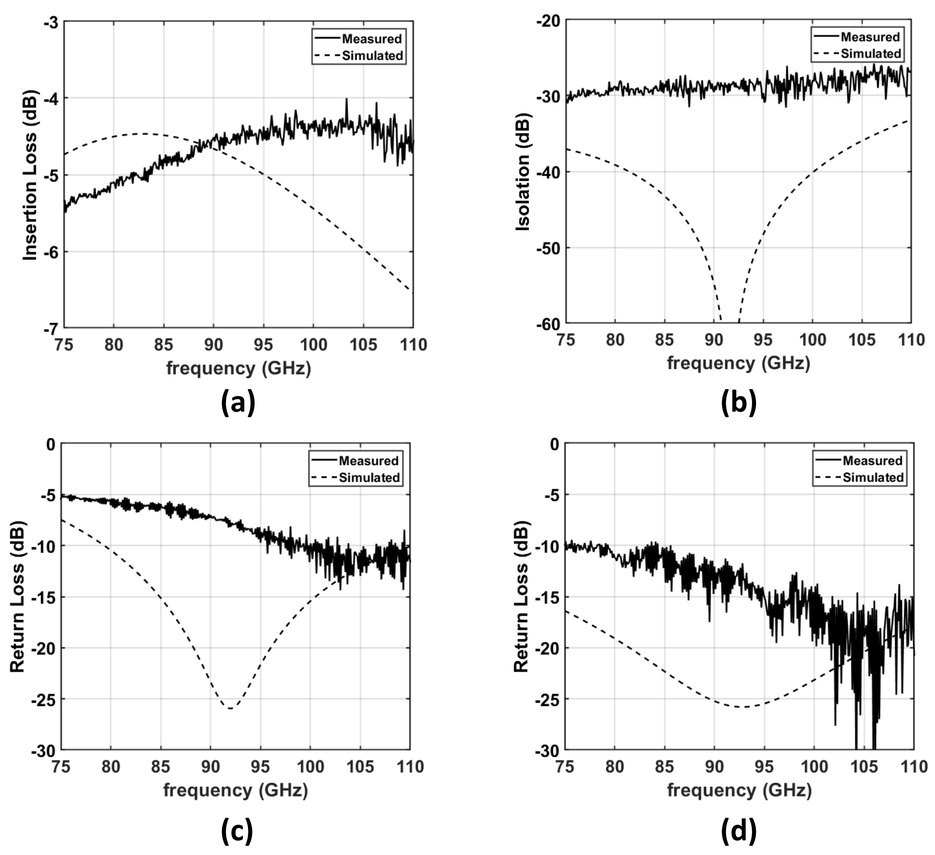

Fig. 4. Measured S-parameters: (a) IL, (b) isolation, (c) S_{11}, and (d) S_{22}.

- 4.3 dB IL @ 100 GHz, >26 dB isolation (W-band)
- Isolation degradation due to parasitic extraction inaccuracies
- 17 dBm simulated IP_{1dB}, 0.012 mm^2 core area

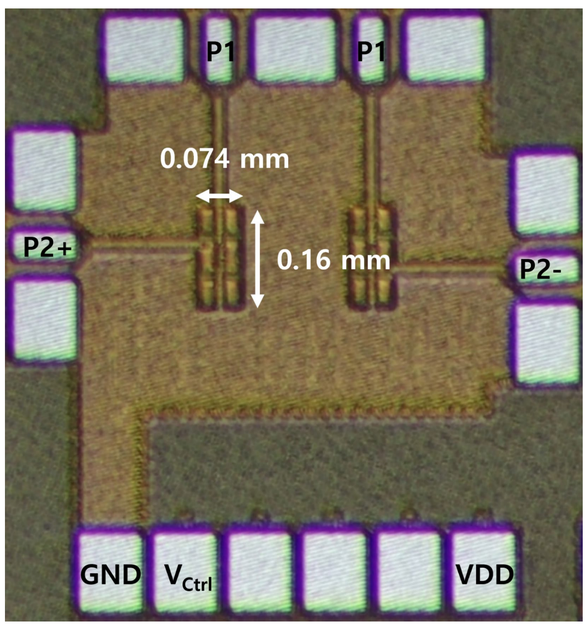

Fig. 5. Chip photograph

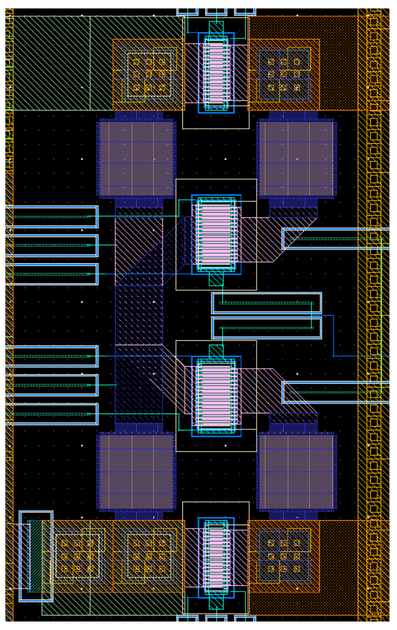

Fig. 6. Core Layout

▪ Reference

[1] J. Hwang, S. Ju and B. -W. Min, "Compact Neutralized SPDT Switch With High Pole-to-Throw and Throw-to-Throw Isolation," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 73, no. 11, pp. 9196-9205, Nov. 2025