IDEC Chip Design Contest

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Design of a 3–30 GHz CMOS True-Time-Delay Circuit for Wideband Phased Array Systems

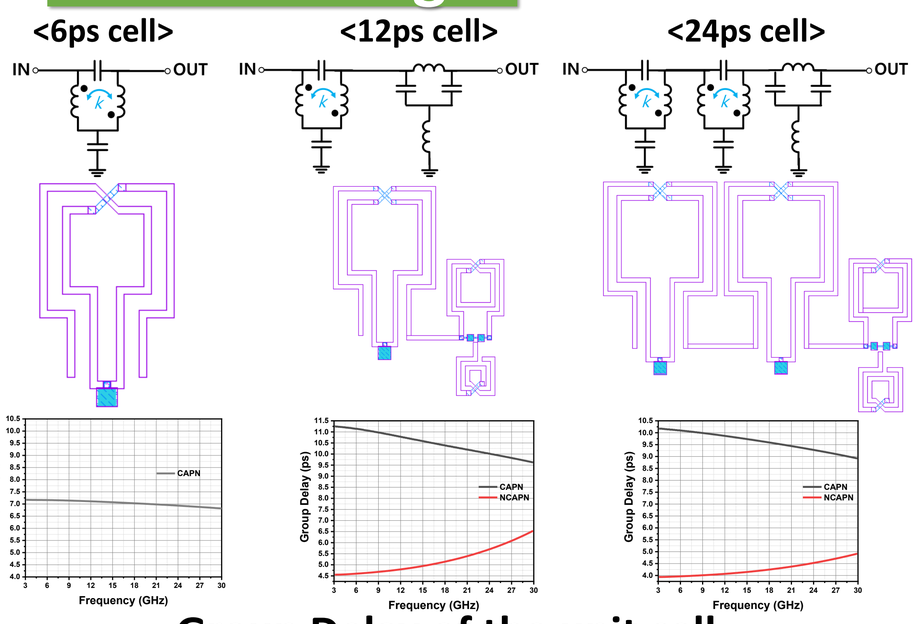
JeongHu Nam and TaeHwan Jang
Hanyang University ERICA

Introduction

- In wideband phased-array systems, conventional phase shifters suffer from beam squint because the equivalent time delay varies with frequency. To address this issue, true-time-delay (TTD) circuits are used to provide frequency-independent delay for accurate wideband beam steering.

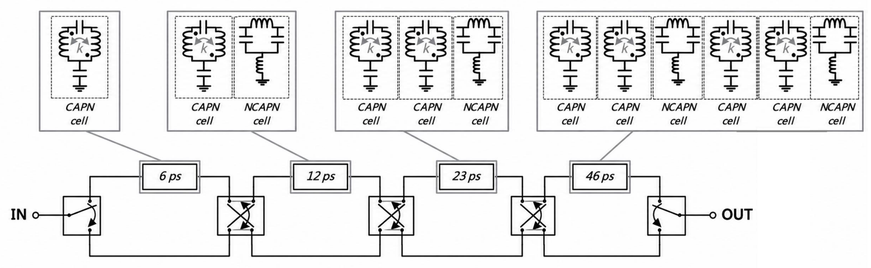
- Among passive TTD structures, transmission lines offer flat group delay but require a large area, while low-pass filters are compact but have limited delay-bandwidth performance. Therefore, this work adopts an all-pass-network-based TTD structure to achieve compact and wideband delay control.

Circuit Design



Group Delay of the unit cell

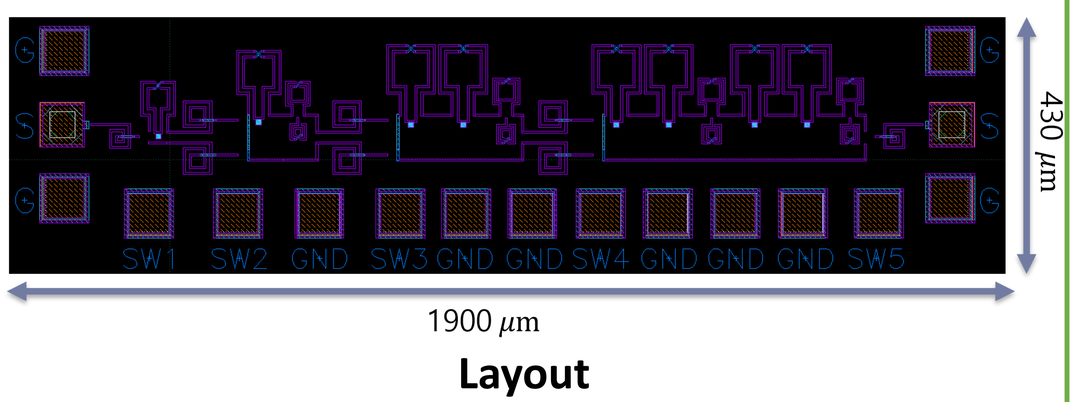
- The proposed TTD circuit is designed for wideband phased-array beamforming over the 3–30 GHz frequency range. To achieve a flat group delay, the delay cell combines CAPN and NCAPN structures, which have opposite group-delay slopes with frequency. By compensating these opposite delay characteristics, the unit delay cell can provide a more stable time delay across the wideband operation.



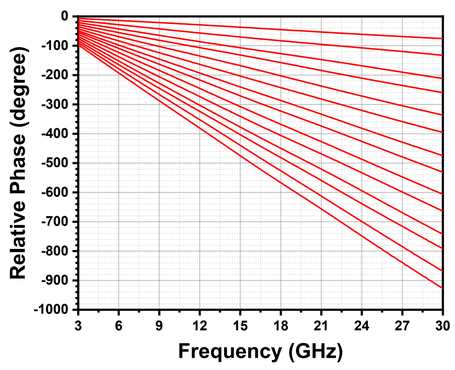
Full - Schematic

- The overall TTD architecture consists of multiple delay cells and SPDT/DPDT switch networks. Each delay cell is first designed to realize the target delay value, and both the delay cells and switches are matched to 50 Ω at the input and output ports. This design approach allows the delay characteristics of each cell to be maintained even after integration with the switch network.

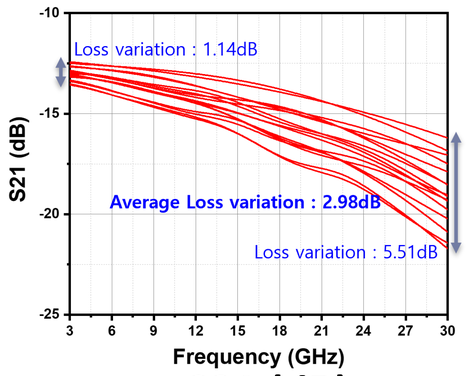
Results



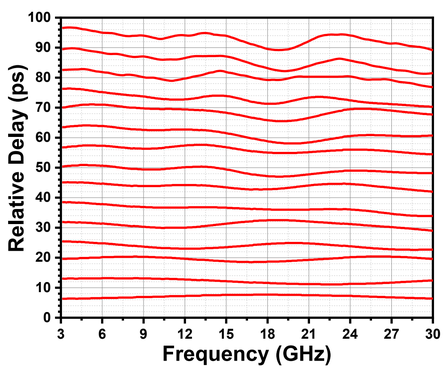
Layout



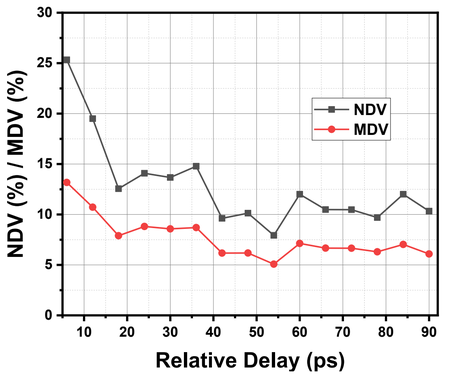
Relative Phase (degree)



S21 (dB)



Relative Delay (ps)



NDV (%), MDV (%)

True – Time - Delay					
Tech	Maximum delay (ps)	Nominal Loss (dB)	DBW	Minimum delay (ps)	Size
28nm CMOS	90	16.8 (13~18.9)	2.43	6	0.43

Conclusion

3-30 GHz CMOS true-time-delay circuit was designed for wideband phased-array beamforming. The proposed architecture combines CAPN and NCAPN all-pass delay cells to compensate frequency-dependent group-delay slopes, while SPDT/DPDT switch networks select the required delay state. Simulation results show a maximum relative delay of 90 ps with a minimum delay step of 6 ps, demonstrating the feasibility of compact wideband TTD implementation in 28-nm CMOS.

Acknowledgement

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