IDEC Chip Design Contest

A Transimpedance Amplifier with Negative Capacitance Compensation for Nanopore Applications

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Introduction

This paper presents a low-noise transimpedance amplifier (TIA) with a parasitic capacitance compensation circuit for nanopore-based DNA sequencing applications. The designed TIA serves as the front-end of the sensing system, where accurate measurement of ultra-small ionic currents is essential. To overcome bandwidth limitations caused by the intrinsic parasitic capacitance of the nanopore, a compensation technique is incorporated into the TIA architecture. The proposed design was implemented using a 180 nm BCDMOS process, and its performance was verified through simulation and analysis. The results demonstrate improved noise performance and bandwidth characteristics, confirming the effectiveness of the proposed compensation scheme. These outcomes indicate that the designed TIA is suitable for high-sensitivity nanopore signal acquisition in DNA sequencing systems.

Block Schematic Architecture

A negative capacitance compensation circuit is designed and implemented to mitigate the parasitic capacitance (Cp) introduced by the nanopore interface, which is one of the primary factors limiting the bandwidth of the sensing system. Figure 1 (b) illustrates the overall circuit architecture for parasitic capacitance compensation. The proposed design employs a negative capacitance structure that generates an equivalent capacitance with opposite polarity to Cp, thereby effectively canceling its effect.

Figure 1 (c) shows the simulated frequency response of the system before and after applying the negative capacitance compensation. When the parasitic capacitance is compensated, the dominant pole associated with Cp is effectively shifted, resulting in an extended bandwidth and improved high-frequency response. This behavior can be analytically explained by the change in the overall impedance of the signal path, where the cancellation of Cp reduces the capacitive loading effect and enhances the frequency response characteristics, as described by the corresponding equation.

$$\omega_0 \approx \frac{2A_0}{C_p R_F} \quad \rightarrow \quad \omega_0 \approx \frac{2A_0}{R_F}$$

Figure 1(d) presents the detailed circuit implementation of the negative capacitance generator. Under appropriate biasing and design conditions, the circuit produces a stable negative capacitance, which effectively counteracts the parasitic component introduced by the nanopore and interface circuitry. The analytical model confirms that the effective input capacitance can be significantly reduced, leading to improved transient response and faster signal settling behavior

$$Z_{in} = -K \frac{1}{j\omega C_{REF}} \quad K = \frac{GBP\, R_1 + (R_1+R_2)\cdot j\omega}{GBP\, R_2 - (R_1+R_2)\cdot j\omega}$$

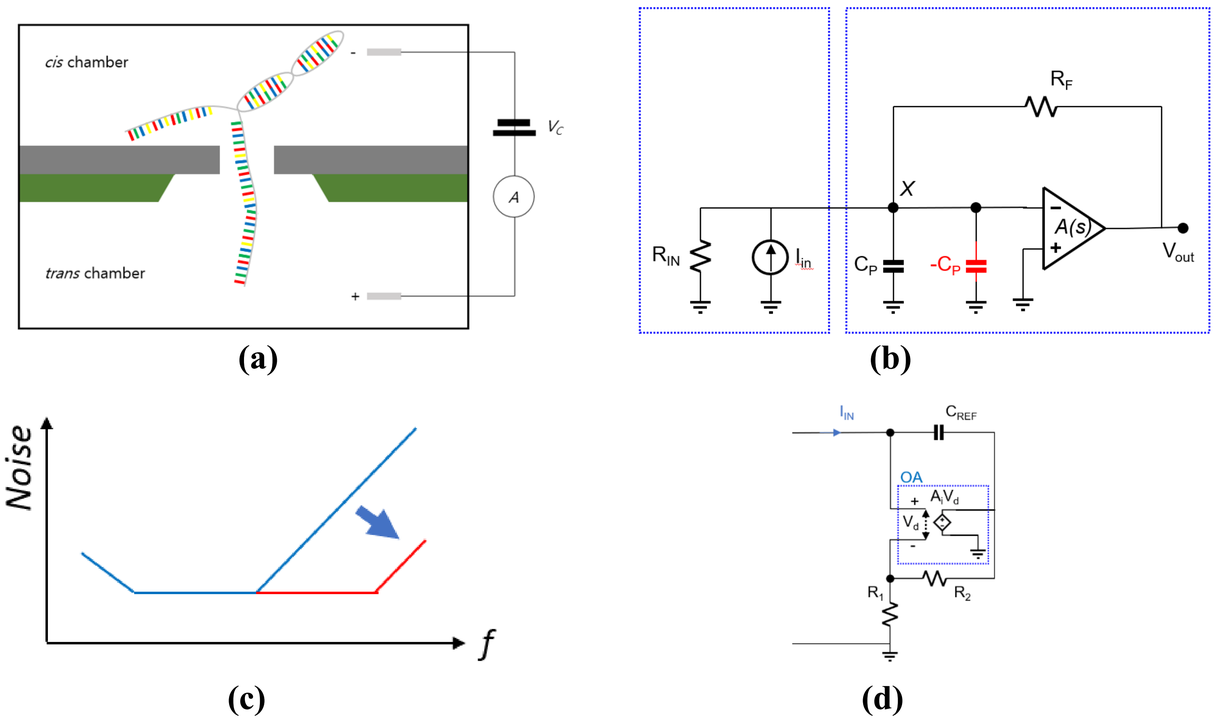

Figure 1. (a) DNA translocating through the nanopore between the cis and trans sides of the chamber **(b)** Negative Capacitance Compensation Circuit used in Nanopores **(c)** Frequency domain changes through the negative capacitance compensation circuit structure (Blue: frequency domain results before applying the negative capacitance compensation circuit structure; Red: frequency domain results after applying the negative capacitance compensation circuit structure) **(d)** Negative Capacitance Compensation Circuit Schematic

Experimental Results

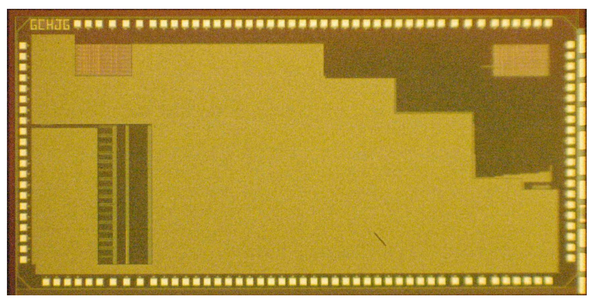

Figure 2. A microscopic image of the chip

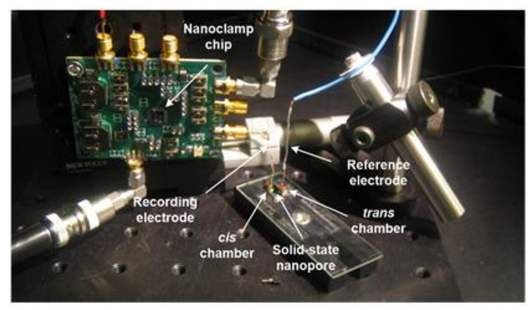

Figure 3. Experimental setup for nanopore experiment

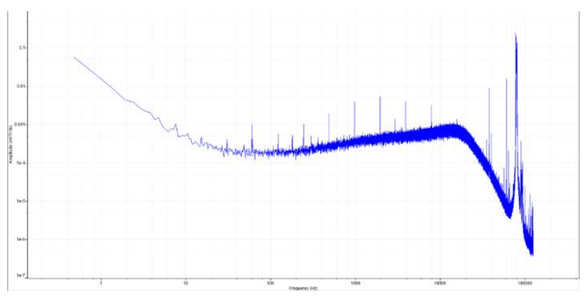

Figure 4. Noise measurement results in the frequency domain

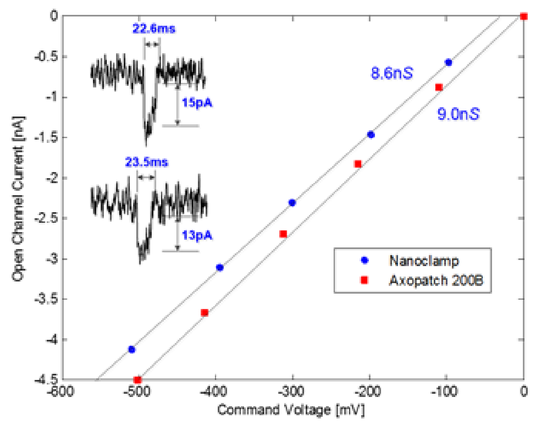

Figure 5. Comparison of I–V characteristics with Axopatch 200B and DNA sensing experimental results

Conclusion

This work presented a low-noise transimpedance amplifier (TIA) incorporating a negative capacitance compensation technique for nanopore-based DNA sensing applications. By effectively mitigating the impact of parasitic capacitance, the proposed architecture achieved enhanced bandwidth and improved signal fidelity while maintaining low-noise performance. The designed system was successfully implemented using the DB HiTek 180 nm BCDMOS process and experimentally validated through frequency-domain noise measurements and nanopore sensing experiments.

The measurement results, including I–V characterization in comparison with the Axopatch 200B and DNA translocation experiments, demonstrated the accuracy and practical applicability of the proposed system. These results confirm that the proposed TIA is a viable solution for high-resolution, low-noise signal acquisition in nanopore-based biosensing systems, and it is expected to contribute to the development of compact and efficient next-generation DNA sequencing platforms.

Acknowledgement

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