TOWERJAZZ
The Global Specialty Foundry Leader

RF CMOS SOI Switch Technology

The TowerJazz RF CMOS SOI switch process combines a 6 or 4 metal layer 0.18µm CMOS process with options for 1.2, 1.8, 2.5V, 3.3V, and 5V transistors. The technology offering is further enhanced by proven RF-switch centric design libraries and world-class design enablement for higher throw-count switches.

Process options include a low-Vt MOSFET, a 5V RFLDMOS device with Ft of 19 GHz and BVDSS of 20V, and passive components including silicided and unsilicided poly resistors, 2 fF/µm and stacked 4 fF/µm metal-insulator-metal capacitors, scalable geometry inductors, and fixed geometry baluns and transformers.

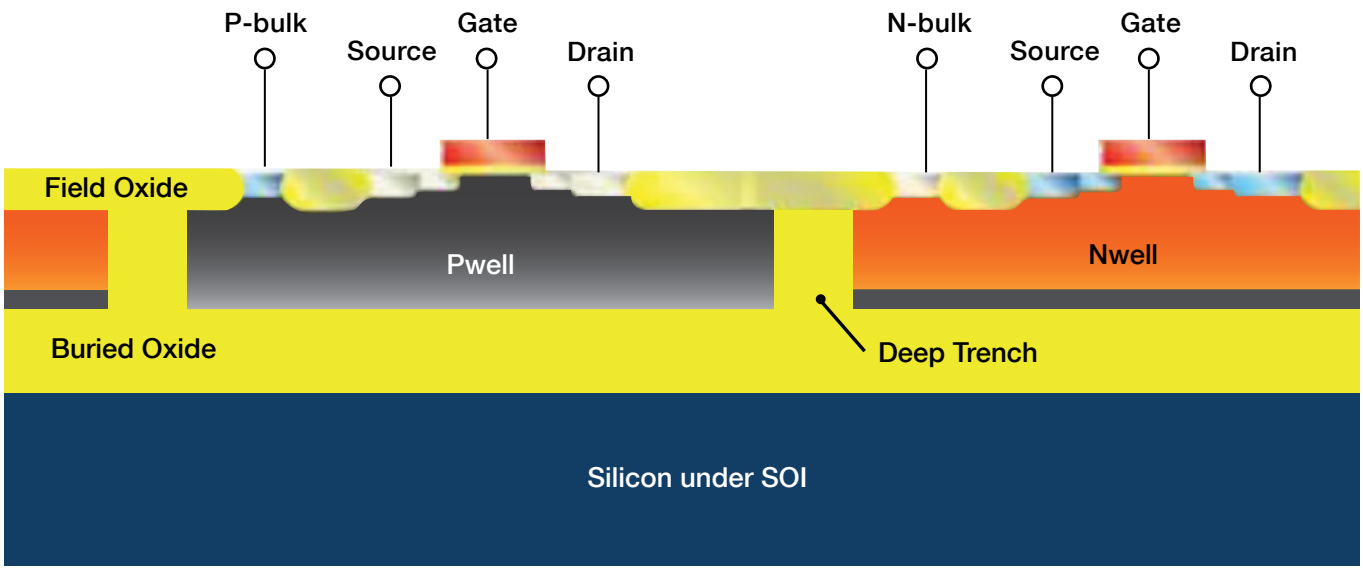
The back end metal is Aluminum with a 2.8µm thick top layer for high Q inductors. Substrate options include “thick-film” for bulk-like behavior of the active MOSFETs, free of floating body effects and “thin-film” for the best Ron-Coff performance. Isolation between device wells and of field areas below sensitive passive components and metal routing is provided by a deep trench to the buried oxide.

These processes are well-suited for technologies requiring isolation such as cellular switches. Excellent channel isolation better than >-40 dBm, insertion loss of <0.47 dB, low harmonics of better than 80dBc at cellular power levels and inter-modulation distortion below -117 dBm have been demonstrated.

RF CMOS SOI Switch Technology

DEVICE	PARAMETER	CA18HB	CA18QC	CS18Q1	CS18Q2	CS13Q1
CMOS	VDD (V)	1.8/5	1.8/3.3	2.5	2.5/5	1.2/2.5
RFLDMOS	–	✓	–	–	–	–
Native NFET	VDD (V)	5	3.3	–	–	–
Resistors	Sheet resistance (ohm/sq.)	6, 310	6, 310, 1000	310, 1000	310, 1000	310, 1000
MiM (Single/Stacked)	Capacitance (fF/µm2)	2/4	2/4	2	2	2
Varactors	P+/nwell (fF/µm2) Mos	1.3 ✓	1.3 ✓	NA	NA	NA
Metal Layers	–	6	4	4	4	4
Top Metal	Thickness (µm)	2.8	2.8	2.8	2.8	2.8
Substrate	Bulk	SOI	SOI	SOI	SOI	SOI

RF CMOS SOI Switch Cross Section



0.18µm CMOS Design Kit Overview

- Scalable models and p-cells for all devices
- Advanced inductor toolbox (JIT)
- Advanced X-sigma corner modeling
- PCM based models

Analog Mixed-Signal Design Kit Features

- Cadence®-based Design Kit
- Cadence® Assura™ DRC/LVS/RCX
- Support for Mentor® Calibre interactive/XRC
- Support for Spectre, ADS (& RFDE), HSPICE simulators
- Includes basic ESD structures

ASIC Library Views and Features

- Standard Cell Libraries
- I/O Libraries
- Synopsys and Cadence ASIC Flows
- Memory Generators

Supported Models

- **MOSFETs**: Scalable BSIM/PSP models, RF extension models, Non-quasi-static PSP models, mismatch, statistical and noise models
- **BJTs**: Gummel-poon models, mismatch and statistical models
- **MIM Caps**: RF models, mismatch and statistical models
- **Resistors**: Mismatch, statistical and noise models
- **Varactors**: Scalable RF and statistical models

Customer Service and Support

- File Exchange for design kits and online documentation
- Online WIP
- Online Tape-Out System
- Online Help Ticket System
- Dedicated Sales and Engineering Support

For more information please visit www.towerjazz.com.